Silicon Single-Electron Devices

Yasuo Takahashi†, Yukinori Ono, Akira Fujiwara, and Hiroshi Inokawa

Abstract

Single-electron devices (SEDs) are attracting a lot of attention as devices for future large-scale integration because of their inherent low power and small size. We have developed a novel method of fabricating small Si single-electron transistors (SETs) called pattern-dependent oxidation (PADOX) and used it to make many kinds of SEDs. The low power consumption of SEDs is useful for logic circuits. In addition, SETs have two unique features that conventional transistors do not have: multi-input gate capability and conductance that oscillates as a function of gate voltage. We exploit these features to achieve complicated functions for logic circuits, such as multiple-valued logic.

1. Introduction

Recent rapid progress in silicon CMOS (complementary metal oxide semiconductor) LSIs (large-scale integrated circuits) has made possible highly sophisticated information processing and communication tools, such as personal computers and cellular phones, which enable us to process a great deal of information. This progress is enabled by the miniaturization of Si MOS transistors, which proceeds according to Moore's law. **Figure 1** shows predicted feature sizes of transistors. Within 15 years, the device size will be on the nanometer order [1]. However, higher levels of integration produce greater power dissipation in a small Si chip. Even now, the power consumption of some microprocessor chips used in personal computers is more than 50 W. This rise in power will suppress further integration, which will limit the functionality of information processing and communication tools. That is to say, the device temperature cannot exceed the cooling limit. In addition, for mobile applications, which are going to become more widespread and important, we must extend battery life [2]. Therefore, we must develop new devices for future information technology that enable us to achieve low power consumption as well as high functionality. Single-electron devices (SEDs) are the key to minimizing power consumption because they can control the transfer of individual electrons [3]-[5]. In addition, such devices have high functionality that conventional transistors do not have; for example, they can support multiple gates and exhibit conductance characteristics that oscillate as a function of gate voltage. We can exploit these special features to achieve high performance with low power dissipation.

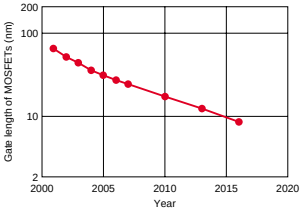

Fig. 1. Gate lengths of MOSFETs predicted in International Technology Roadmap for Semiconductors [1].

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2. Single-electron transistor (SET)

The most primitive SED [6], [7] has a simple three-terminal structure, as shown in **Fig. 2**. The device must have a small island together with a gate electrode coupled to the island with gate capacitance C_g. Source and drain electrodes are attached to the island via a tunnel barrier. Due to the three-terminal structure, we call this device a single-electron transistor (SET).

The operating principle of the device is based on the balance of charge between the gate electrode and the island. When the source and drain terminals are grounded for simplicity, and when a voltage V_g is applied to the gate, charge C_gV_g accumulates in the gate electrode. However, since tunnel barriers isolate the island from the source and drain, the number of electrons in the island should be a fixed integer. The total charge in the island $-Ne$, where N is the number of electrons and e the elementary charge, is balanced with that in the gate when $C_gV_g = Ne$ is satisfied. In this condition, the number of electrons is stable, so N cannot change. That is, current does not flow through the SET island. This is the Coulomb-blockade condition. As the gate voltages increase, the total charge in the gates increases, and the charges become unbalanced. Then, when $C_gV_g = (N+1/2)e$, the electrostatic potentials of two states (for N and for N+1 electrons) become equal, which means that the island can contain either N or N+1 electrons. Therefore, electrons flow one at a time when a small voltage is applied between the source and drain electrodes. The number of electrons in the island is N+1 after a single electron tunnels from the source to the island. The number returns to N after an electron tunnels from the island to the drain. When this sequence is repeated, a current due to single-electron tunneling flows. If the gate voltages increase further, the number of electrons becomes stable at N+1. As a result, the source-drain conductance oscillates as a function of gate voltages, as shown in **Fig. 3**.

For a SET to operate at high temperature T, the island should be small to maintain the Coulomb blockade condition, i.e., $e^2/(2C_{total}) > 3.5\ kT$, where C_{total} is the total capacitance of the SET island. The SET island must be smaller than 10 nm for room-temperature operation. The most difficult issue in fabricating such a SET is attaching two tunnel capacitors to the nanometer-scale island. We have already developed a controllable fabrication method called pattern-dependent oxidation (PADOX) [8]-[10], which converts a small Si wire pattern on an SOI (silicon on insulator) wafer into a single-electron island with a tunnel capacitor at each end. In this method, special phenomena that occur during the oxidation of Si nanostructures on SiO_2 play a crucial role.

3. SET fabrication by PADOX

The operating principle of the SET allows us to use any conductive material—metal or semiconductor—as a base material. Among the available materials, silicon is one of the best candidates because we can utilize sophisticated fabrication processes developed for recent CMOS LSIs. In addition, the Si/SiO_2 system is the most reliable one, as demonstrated in Si LSIs.

PADOX [8]-[10] uses thermal oxidation, which is well known as the most dependable and simplest method of obtaining a stable Si/SiO_2 interface. The initial structure of the SET is a narrow, short one-dimensional Si wire fabricated on a thin SOI wafer as shown in **Fig. 4**. The typical wire width is about 30 nm. The wire height, which is the thickness of the SOI layer, is also about 30 nm. The wire length is varied to control the island size. The SET fabrication mechanism is as follows. When a narrow Si wire is thermally oxidized in dry oxygen ambient, the oxidation is suppressed due to the huge stress accumulated

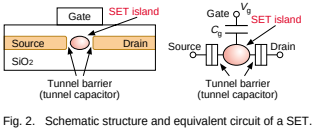

Fig. 2. Schematic structure and equivalent circuit of a SET.

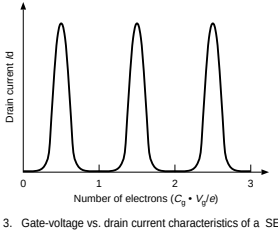

Fig. 3. Gate-voltage vs. drain current characteristics of a SET.

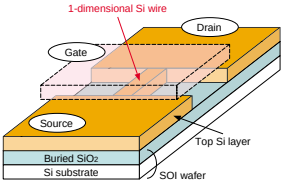

Fig. 4. Initial device structure of the SET before PADOX.

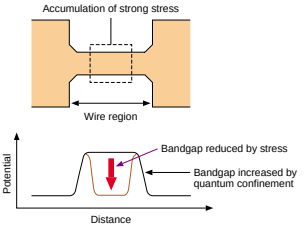

Fig. 5. Schematic plane view of the device and potential diagram along the Si wire.

in the grown SiO_2, which completely surrounds the wire. It has been reported that a compressive stress larger than 20,000 atm accumulates in the SiO_2 when a 10-nm-diameter Si wire is formed by oxidizing a 30-nm-diameter Si wire [11]. When the Si wire structure shown in Fig. 4 is subjected to thermal oxidation, a compressive stress is exerted on the middle part of the wire. The 20,000-atm stress produces strain in the wire and reduces the bandgap by about 150 meV. This reduction cancels out the effective bandgap increase of about 50 meV due to the quantum size effect in a 5–10-nm Si wire [12], [13]. As a result, the potential profile is as schematically shown in **Fig. 5**. The two potential hills serve as tunnel barriers: a tunnel capacitor is formed between the Si island and the wider Si layer. This mechanism enables us to make a SET in a self-aligned manner.

The typical electrical characteristics of an Si SET fabricated by PADOX are shown in **Fig. 6**. The conductance or current varies depending on the number of electrons in the SET island, which is different from the characteristics shown in Fig. 3. The reason is as follows. In the case of SETs fabricated from a semiconductor, since there are only a few electrons in the island, the wave function distribution changes according to the number of electrons, which affects the tunnel resistance. This is one of the phenomena in a few-electron regime. It is quite interesting to investigate SETs from the physics viewpoint because quantum effects play an important role in 10-nm-sized Si islands [14]. In this report, however, we focus on the device application of SETs.

It has generally been said that the greatest drawback of SETs is that the operating characteristics sometimes change due to the offset charge effect. However, SETs fabricated by using Si MOS processes are definitely stable against long-term drift, which

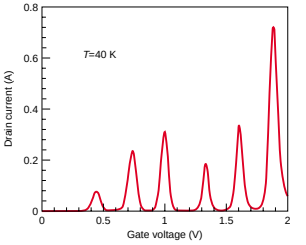

Fig. 6. Drain current vs. gate-voltage characteristics measured at drain voltage of 1 mV.

is essential if they are actually to be used [15], [16]. We have confirmed that the characteristics shown in Fig. 6 did not change over a seven-year period. This is the great advantage of Si SETs [7].

4. Logic circuit application of SETs

SEDs have two main applications: memory and logic circuits. Since their most prominent feature is low power operation, the application to logic circuits seems the most promising. Low power operation is essential to future logic LSIs, in which power dissipation will limit integration levels. In addition, devices for future LSIs should be small to achieve a high integration density as well as low power consumption [7]. As discussed above, the operating principle based on the Coulomb blockade allows the

device to operate more stably as it becomes smaller. This is the opposite of the situation in MOSFETs, where a smaller size creates undesirable characteristics, such as punch through or gate leaks.

In addition, SETs have several other special features that conventional transistors (MOSFETs and bipolar transistors) do not have. As described above, the drain current or conductance shows oscillatory characteristics according to the number of electrons in the island. Another special feature is that the operating principle lets the device support multiple gates. Some SET logic circuits fabricated using PADOX, in which these features are exploited, are discussed below.

4.1 Multigate SET

SETs inherently have multiple gates as shown in the equivalent circuit in **Fig. 7**. Each gate electrode couples directly to the SET island with gate capacitance C_{gi}. As described in section 2, since the total charge accumulated in gates is $\sum C_{gi}V_{gi}$, the drain current oscillates as a function of $\sum C_{gi}V_{gi}$. These characteristics give SETs two special features. One is that the source-drain current is determined by the sum of the products of each gate capacitance C_{gi} and gate voltage V_{gi}. The other special feature of the SET is oscillatory characteristics. The periodically oscillating current characteristics are useful to achieve periodical functions, such as adder or parity check circuits, which are widely used in current logic circuits. As described in section 2, the drain current is minimum when the sum $\sum C_{gi}V_{gi}/e$ is an integer. Conversely, when the sum is a half integer, the current is maximum. Conventional devices do not have these kinds of features.

If all gate capacitances (C_{gi}) of the SET are the same C_{g0}, and if we use an input voltage (V_{gi}) for high-level $e/(2C_{g0})$, we can obtain the functions of a multi-input exclusive-OR gate. Each high input-gate can switch the current level from high to low and vice versa. This means that an even number of "HIGH" gates creates the "LOW state" and an odd number creates the "HIGH state". This is exactly the function of the Exclusive-OR (XOR) gate in a binary logic circuit. We fabricated such a device having two equal gates [17]. SEM images of the device are shown in **Figs. 8(a)** and **(b)**. A small one-dimensional Si wire fabricated on an SOI wafer (Fig. 8(a)) was converted into a small SET by PADOX. Then, using an electron-beam exposure system with a high overlay accuracy, we attached two ultrafine poly-Si gates so as to cover part of the island as shown in Fig. 8(b). The

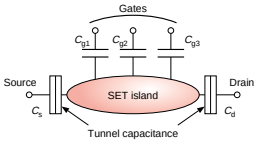

Fig. 7. Equivalent circuit of a multigate SET.

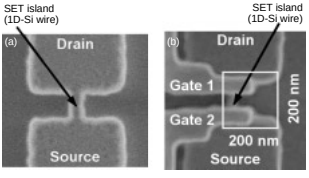

Fig. 8. SEM image of a dual gate SET before (a) and after (b) the formation of two ultra-fine gate electrodes.

capacitances of the two gates were almost equal due to the symmetrical configuration. The drain current oscillation characteristics as a function of one of the gate voltages are shown in **Fig. 9(a)**. Since both gates have almost the same capacitance of 0.4 aF, the oscillation phase shifts by about π in the negative voltage direction when one of the gate voltages V_{g2} is changed from 0 V to 0.2 V. **Figure 9(b)** shows the drain current switching measured at 40 K in response to the switching of the two input-gate voltages (V_{g1} and V_{g2}) between 0 and 0.2 V. Low current levels were obtained only when the input voltages were both high or both low. This represents an XOR-gate operation, which can be implemented with just one SET.

This functionality of the multigate SET enables us to make multibit adders with a small number of transistors without any wire crossing [18]. This is advantageous not only for reducing device area but also for achieving high-speed operation, despite the low drivability of SETs.

4.2 Multiple-valued operation

It is widely known that multiple-valued logic allows us to reduce the number of transistors and the amount of wiring in LSIs. This is another effective way to reduce the power dissipation and chip size of

LSIs. SETs, which have oscillatory conductance characteristics, are highly suitable for multiple-valued applications [19], [20], in which the number of electrons in the island represents multiple values. To achieve several stable points, we must attain multi-peak negative differential resistance (NDR) characteristics in which the current oscillates as a function of drain voltage. As shown in Fig. 6, the SET current oscillating as a function of input gate voltage cannot be used for a multiple-valued operation, because the SET cannot generate output voltages proportional to the number of electrons in the SET island. The problem is that the Coulomb blockade is lifted when V_{ds} is higher than e/C_{total}, which limits the voltage V_{ds} that can be applied to the drain terminal.

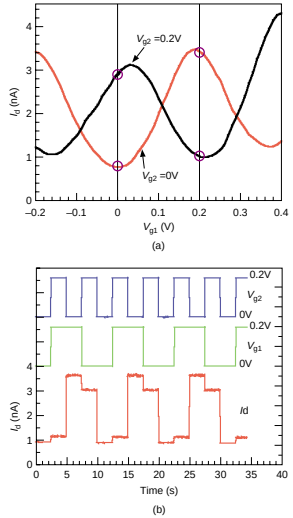

Fig. 9. Drain current I_d vs. gate voltage characteristics of a dual gate SET (a) and drain current switching characteristics (b).

To overcome this problem, we developed a SET-MOSFET combined circuit. We can convert the horizontal axis of current characteristics oscillating as a function of gate voltage to ones oscillating as a function of drain voltage by connecting a small MOSFET in series with the SET. One of the great advantages of the PADOX method is that the basic fabrication process is compatible with that for conventional MOSLSIs, which enables us to easily combine SETs and MOSFETs [19]. The equivalent circuit of the device is shown in **Fig. 10(a)**. The gate of a SET is connected to the drain of a MOSFET. The MOSFET connected in series keeps the V_{ds} at nearly $V_{gg} - V_{th}$, where V_{th} is the threshold voltage of the MOSFET. If $V_{gg} - V_{th}$ is set lower than e/C_{total}, clear current oscillation can be retained even when a higher voltage V is applied at the drain of the MOSFET. By connecting the SET gate to the MOSFET drain, we obtain multi-peak current oscillation as a function of V, resulting in NDR characteristics such as those schematically shown in **Fig. 10(b)**.

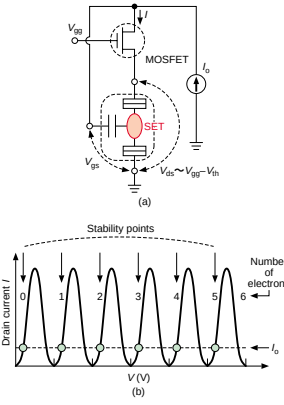

Fig. 10. Equivalent circuit composed of a MOSFET and SET (a) and schematic two-terminal *I-V* characteristics of the circuit (b).

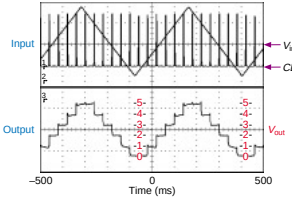

Fig. 11. Measured quantizer operation. The operating speed is not limited by the intrinsic performance of the device, but by the large capacitance existing at V_{out}.

If a current source I_0 is connected to the circuit, many points (indicated by arrows in Fig. 10(b)) become stable. Each stability point corresponds to the number of electrons in the island at a particular applied voltage V. It is advantageous that just two transistors can provide a multipeak NDR device in which the number of the peaks is infinite in principle within the breakdown voltages of the MOSFET drain or the SET gate. These characteristics can also be applied to multiple-valued memories [19], [21]. In conventional multipeak NDR devices, such as resonant tunneling diodes, the same number of devices as peaks is required.

The most important use of this NDR device with multiple stability points is to build multiple-valued logic circuits. One of the basic circuits of multiple-valued logic is a quantizer that discriminates an analog input signal into predefined voltage levels. By using the circuit shown in Fig. 10(a), we have built a quantizer [18]. **Figure 11** shows measured waveforms for V_{in}, CLK, and V_{out} of the quantizer. Input triangular wave V_{in}, transferred to the drain terminal (V in Fig. 10(a)) according to short clock pulses (CLK), settles down to the stability points, and output voltage V_{out} is quantized to the levels 0–5, as shown in the figure. This demonstrates the operation of a quantizer with a six-valued output voltage. Although the operating speed is rather slow, it is not limited by the intrinsic performance of the device, but by the large capacitance existing at the V_{out} terminal for the measurement with an oscilloscope. Based on the circuit shown in Fig. 10(a), we have proposed a full adder for redundant number representation with a very small number of transistors, and a high-speed analog-to-digital converter [21]. These are advantageous not only for circuit size reduction but also for low-power operation.

5. Conclusion

Single-electron transistors (SETs) have high potential for future large-scale integration because of their low power consumption and small size. Although it is not easy to fabricate them because of their small size, we have developed a novel fabrication method for Si SETs called pattern-dependent oxidation (PADOX), which is simple and compatible with the conventional fabrication processes for CMOS LSIs. We have demonstrated some logic-circuit applications of devices fabricated by PADOX. In these applications, we use the special functional features of the SET, such as multiple-gate capability and multiple-peak oscillatory characteristics. By exploiting these special features, we can achieve complicated functions with a small number of transistors, which will reduce the size and power dissipation of circuits.

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