

Packet-level Optical Timing-pulse Generator and Its Application to 40-Gbit/s Optical Packet Self-routing

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Abstract

We describe a novel packet-level optical timing-pulse (clock-pulse) generator that generates one optical pulse per incoming asynchronous burst optical packet: the generated optical pulse is accurately synchronized with the input optical packet. We also describe 40-Gbit/s optical packet self-routing based on 40-Gbit/s 16-bit serial optical-label recognition by a CMOS (complementary metal-oxide-semiconductor) circuit operated together with an all-optical serial-to-parallel converter and the optical timing-pulse generator.

1. Introduction

Optical packet switching is a promising way to meet bandwidth requirements as they increase with the rapid growth of Internet traffic, because it enables the maximum utilization of a single channel provided in the optical network [1]. The fundamental functions of a switching node in such an optical packet-switched network are burst-mode synchronization, recognition of the optical label attached to each packet and label-based packet forwarding of incoming high-bit-rate burst optical packets. For both the label recognition and packet forwarding control, the label refers to a routing table listing many addresses and corresponding route information. The execution of these rather complicated label processing functions is inevitably entrusted to electronic circuits, especially CMOS LSIs (complementary metal-oxide-semiconductor circuits on large-scale integrated circuits). However, it is difficult to process serial-bit signals, especially asynchronous burst ones, that have a bit rate of 40 Gbit/s or higher directly with such electronic circuits because of their limited operating speed. Therefore, a method of interfacing high-bit-rate burst optical packets with a smart but rather slow

electronic label processor is essential. The self serial-to-parallel conversion (self-SPC^{*1}) system shown in Fig. 1 provides such an interface in the optical domain. The self-SPC system consists of an all-optical serial-to-parallel converter (SPC) [2], [3] and a packet-level optical timing-pulse (clock-pulse) generator (OCG) [4]. When a high-bit-rate asynchronous burst optical packet arrives, the self-SPC system converts the *n*-bit serial optical label attached to the optical packet into *n* parallel channels of signals by operating its all-optical SPC once per packet. For this operation, the OCG feeds one synchronized control signal to the SPC per packet. Because the bit rate of the parallelized label signals is as slow as the packet rate, the parallel signals can be processed by a rather slow CMOS circuit after they have been converted into electrical signals with an appropriate duration by a slow photodetector (PD) array. The self-SPC system can thus decrease the bit rate of high-bit-rate burst optical packets and interface them with a CMOS-based label processor that enables overall and systematic control of the packet switching.

In this paper, we describe a novel OCG composed of optoelectronic circuits [4]. The OCG detects an incoming asynchronous burst optical packet of arbitrary length that does not have any preamble bits and

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*1 SPC: refers to both a serial-to-parallel converter and the process of serial-to-parallel conversion.

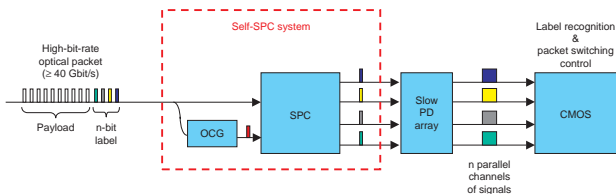


Fig. 1. Self-SPC system for processing high-bit-rate optical labels.

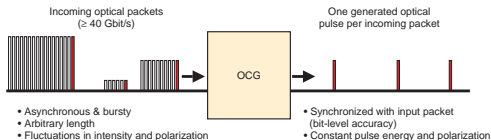


Fig. 2. Operating functions of the packet-level optical timing-pulse (clock-pulse) generator (OCG).

generates one optical pulse per packet. The generated optical pulse is accurately synchronized with the leading pulse of the input packet. We also describe a self-routing scheme for 40-Gbit/s burst optical packets [5], [6], which is constructed using the self-SPC system as an interface for 40-Gbit/s optical labels with a CMOS label processing circuit.

2. Packet-level optical timing-pulse (clock-pulse) generator (OCG)

Figure 2 shows a schematic diagram of the operating functions required for an OCG. An OCG must detect burst optical packets and generate one optical pulse per packet. The output optical pulse must be accurately synchronized with the input packet [4], [7], [8]. Some fluctuation of the intensity and polarization of input packets is inevitable. Asynchronous packets with arbitrary lengths should be detected [4], [7]–[9] and output pulses should have constant energy and polarization. The most important requirement is that the optical-pulse generation must be on a packet-by-packet basis, but the generated optical pulse must have bit-level timing accuracy.

Figure 3 shows the optoelectronic circuit we have

developed as the OCG [4]. It is composed of an optical-to-electrical (OE) converter, which generates a single electrical pulse synchronized with an input packet, and an EO converter, which is a gain-switched² distributed feedback laser diode (DFB-LD) driven by the OE converter. The OE converter consists of i) a photoconductive sample-and-hold (S/H) circuit, which generates an electrical step signal by detecting the leading pulse of the input packet, ii) an optical receiver, which provides the S/H circuit with set and reset signals, and iii) a pulse generating circuit, which transforms the step signal into the single output electrical pulse. The S/H circuit consists of a metal-semiconductor-metal photodetector (MSM-PD), a hold capacitor, a high electron mobility transistor (HEMT) buffer circuit, and a resetting transistor. The optical receiver has a rather slow response time, so that it can generate an output signal in response to the leading '1' bit of an incoming optical

² Gain switching is a popular method of driving a semiconductor LD to generate a short optical pulse. Using the phenomenon of relaxation oscillation induced in an abruptly switched-on LD, we can obtain an optical pulse with a duration shorter than that of the driving current-pulse from the driven (gain-switched) LD.

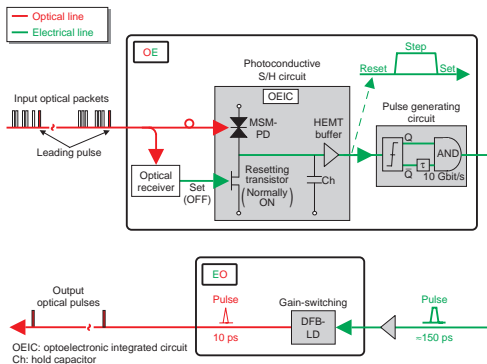


Fig. 3. Optoelectronic circuit for the OCG.

packet and keeps generating it for the whole packet duration without responding to any '0' bits included in the packet. Thus, it generates one rectangular electrical signal per incoming packet. (An IP (Internet protocol) packet never has more than eight continuous '0' bits. Thus, an optical receiver having a response time longer than a few bytes can operate correctly as mentioned above, provided the guard-band length is longer than the response time so that the output signal disappears during the guard band.) When there is no incoming optical packet, the S/H circuit is always reset. (The resetting transistor is normally on and short-circuits the hold capacitor.) When a packet arrives, the optical receiver receives a split input packet a moment earlier than the S/H circuit does, and this sets the S/H circuit. (The electrical signal generated by the optical receiver switches off the resetting transistor to make it possible for the hold capacitor to hold a charge.) Then, the split identical packet with a slight delay launched into the S/H circuit induces a charge in the MSM-PD by its leading pulse and the S/H circuit generates a step-like electrical signal by holding the charge in the hold capacitor. The step signal is then transformed to an electrical pulse about 150 ps wide by the pulse generating circuit, which detects the rising edge of the S/H output.

Here, the pulse width is adjusted by an electrical delay (τ) in the pulse generating circuit so that it is suitable for the gain switching of the following DFB-LD. By inputting the electrical pulse to the DFB-LD, a single optical pulse having a width of about 10 ps and constant pulse energy and polarization can be obtained from the gain-switched LD. When the packet leaves, the set signal sent from the optical receiver disappears during the guard band before a subsequent input packet arrives, resulting in leaking of the held charge (resetting of the step signal). The OCG thus outputs a single optical pulse synchronized with the leading pulse of the input packet. It can accept burst optical packets that do not contain any preamble bits for clock extraction because it detects only the leading pulse. For the same reason, it can operate regardless of the input packet bit rate. In addition, it can detect arbitrarily long asynchronous packets because the set/reset function is controlled by the input packet itself.

Figure 4(a) shows the waveforms of electrical pulses obtained from the pulse generating circuit (after the pulses were amplified to $6.5 V_{pp}$ to drive the DFB-LD). The measurement was done using 1.543- μm optical pulses with a 2-ps full width at half maximum (FWHM). The parameter was input optical

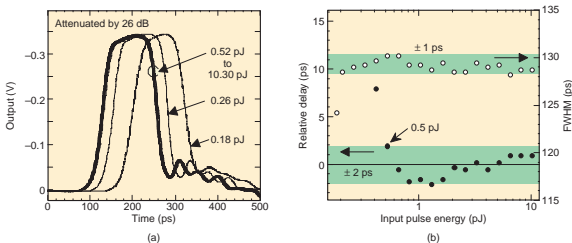


Fig. 4. (a) Waveforms of electrical pulses generated in the OCG (parameter: input optical-pulse energy) and (b) relative delay and FWHM dependencies on input pulse energy.

pulse energy. A unique 130-ps FWHM single electrical-pulse waveform having the same voltage swing and timing was obtained when the energy of the leading pulse of the input packet was larger than 0.5 pJ. (The pulse width was adjusted to match the DFB-LD used in the experiment.) The waveform also exhibited fast rise and fall times of less than 50 ps due to the use of 10-Gbit/s GaAs integrated circuits (ICs) for the pulse generating circuit (Fig. 3), which is fast enough to be applied to the gain switching of the DFB-LD. **Figure 4(b)** shows the input pulse energy versus output relative delay and FWHM of the generated electrical pulses. The variation of the delay was within ± 2 ps when the input energy was larger than 0.5 pJ, even when the input energy was changed by more than 10 dB. The fluctuation of the pulse width was within ± 1 ps. **Figure 5** shows auto-correlation traces measured for the output optical pulses from the OCG. As shown by the dashed line, a 9.2-ps FWHM (assuming Gaussian waveforms) was achieved, which can be applied to 40-Gbit/s systems as described in section 3. The solid line shows the trace for output pulses to which linear chirp compensation was applied for pulse compression. In this case, a 3-ps FWHM was achieved, which can be applied to systems operating at higher bit rates.

The OCG can thus generate one optical pulse per incoming optical packet. The generated optical pulse has bit-level timing accuracy within ± 2 ps. The OCG features high input sensitivity and tolerance for input polarization and power. These features come from the OEO configuration. It can detect arbitrarily long

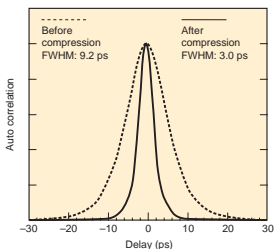


Fig. 5. Auto-correlation traces of optical pulses generated by the OCG.

asynchronous burst optical packets with no preamble bits because its operation is based on leading pulse detection and because the set/reset function is controlled by the input packet itself.

3. 40-Gbit/s optical packet self-routing

In this section, we describe self-routing of 40-Gbit/s burst optical packets [5], for which the self-SPC system is used as an interface for 16-bit serial-bit optical labels with a CMOS label recognition circuit. **Figure 6** shows the experimental setup. Each of the 1.543- μm , 2-ps-FWHM optical pulses launched from a passively mode-locked fiber-laser with a rep-

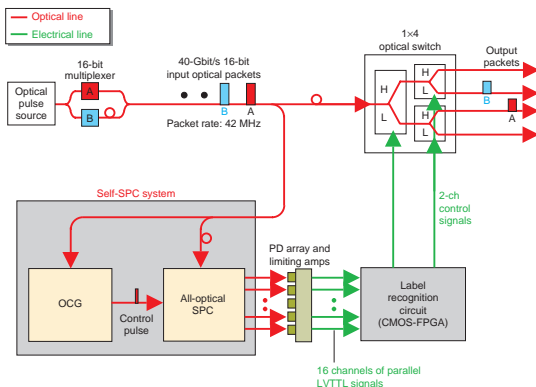


Fig. 6. Setup for 40-Gbit/s 16-bit label recognition and 1x4 self-routing.

etition rate of 21 MHz was split into two and then converted into two different 16-bit optical packets A (1001011011010010) and B (1000111001110001) using PLC-based multiplexers (PLC: planar light-wave circuit). The bit separation in the two packets was 25 ps (corresponding to 40 Gbit/s). These packets were combined to create an input packet stream consisting of the two alternating packets at a packet rate of about 42 MHz. In the experiment, we assigned all 16 bits in each packet to the label and assumed an empty payload. The packet stream was split into two, with one launched into the self-SPC system for label recognition and the other into a 1x4 routing switch. The self-SPC system consisted of the OCG [4] described in section 2 and a 40-Gbit/s 16-ch all-optical SPC [2], [3]. The OCG generates a 10-ps optical pulse synchronized with the input packet. The generated optical pulse has well-defined polarization as well as constant timing and energy, making it very suitable as a control pulse (pump pulse) of the all-optical SPC.

The 16 parallel output signals from the self-SPC system were converted to low-voltage transistor-transistor-logic (LVTTTL) electrical signals (3.3 V) using a 16-ch PD array and limiting amplifiers with

response bandwidth of 155 MHz. They were then input to a CMOS label recognition circuit made with a field programmable gate array (FPGA). **Figure 7** shows the functions of the CMOS circuit operated with the self-SPC system. The circuit checks the input 16-ch signals against a programmable routing table encapsulated in the circuit and generates 2-ch LVTTTL signals for control of the packet forwarding according to the result. The control signal has an NRZ-like waveform, which is held until a subsequent input packet arrives, and is switched quickly enough (in about 3 ns) to allow a short guard band between packets (NRZ: non-return-to-zero). The 2-ch control signals are then input to the 1x4 routing switch, which consists of three 1x2 LiNbO_3 switches in a two-stage configuration.

Figure 8 shows a photograph of a fabricated 40-Gbit/s 16-bit optical-label recognition module. It consists of the all-optical SPC, the PD and limiting amplifier arrays, and the CMOS label recognition circuit. These components are mounted on a printed circuit board that is 15 cm x 8 cm. The module has two optical input ports: one for the 40-Gbit/s optical signal to be converted to parallel signals and the other for the control pulse (pump pulse). The module also

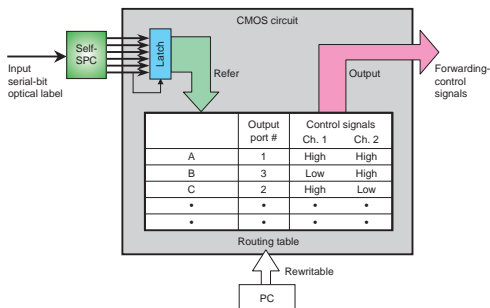


Fig. 7. Functions of CMOS circuit operated using the self-SPC system.

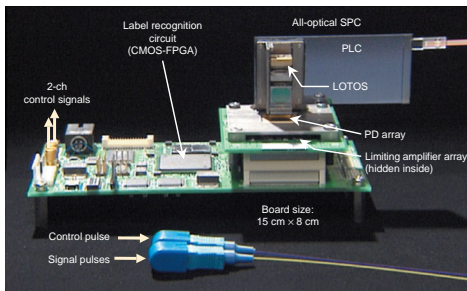


Fig. 8. 40-Gbit/s 16-bit optical-label recognition module.

has two electrical output ports that output the 2-ch forwarding control signals. Using the module, the OCG, and the 1×4 optical switch, we performed a self-routing experiment. **Figures 9(a), (b), and (c)** show the input packet stream, 2-ch forwarding control signals, and output packets from the 1×4 switch, respectively. When the routing table was set to produce the 2-ch control signals of HH and LH (H: high, L: low) for packets A and B, respectively (setting (i)),

we obtained the correct control signals (left side of Fig. 9(b)), and packets A and B were successfully self-routed to the appropriate ports (ports 1 and 3) of the four output ports, respectively (left side of Fig. 9(c)). Furthermore, when the routing table was rewritten by an external computer to produce LH and HL for packets A and B, respectively (setting (ii)), the output ports of packets A and B were correctly changed to ports 3 and 2, respectively (right side of

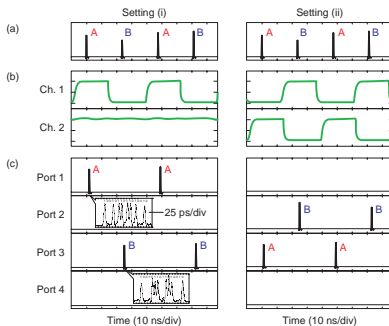


Fig. 9. Results of 40-Gbit/s optical packet self-routing. (a) Input packets, (b) control signals, (c) output packets.

Figs. 9(b) and (c)). We thus experimentally confirmed that the CMOS circuit recognized the 16-bit label for each incoming 40-Gbit/s burst optical packet, generated control signals matched to the routing table, and forwarded the packets to the correct output ports. The processing time (from label input to control signal output) of the CMOS circuit used here is about 20 ns. It should be possible to expand the number of addresses in the routing table against which the input label is checked in one try to more than 1000 without much additional processing time even if a commercially available FPGA is used.

4. Conclusion

We have developed a novel packet-level optical timing-pulse (clock-pulse) generator (OCG) for self serial-to-parallel conversion (self-SPC). The OCG can detect a high-bit-rate arbitrarily long asynchronous burst optical packet with no preamble bits, regardless of its bit rate, and generate one optical pulse per packet. The generated optical pulse is accurately synchronized with the leading pulse of the input packet with timing accuracy within ± 2 ps. The OCG features high input sensitivity and tolerance to input polarization and power (>10 dB) as well as constant output polarization, power, and delay. We have also achieved 1×4 self-routing of 40-Gbit/s burst optical packets by using the self-SPC system. The system

decreases the bit rate of attached 16-bit serial-bit optical labels and thus interfaces them with a CMOS label recognition circuit. 40-Gbit/s optical packets were successfully self-routed to the appropriate output ports as a result of correct label recognition of each optical packet according to a programmable routing table. The self-SPC system acts as an interface between high-bit-rate optical packets and electronic circuits that can achieve a wide variety of functions. It is promising for implementing fast intelligent switching nodes in optical packet-switched networks.

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