Parallel-to-serial Converter Using Metal-semiconductor-metal Photodetectors and Its Application to Bypass/drop Packet Switching

Kiyoto Takahata†, Hirokazu Takenouchi, Tatsushi Nakahara, and Ryo Takahashi

Abstract

We present a parallel-to-serial converter (PSC) for high-speed optical packet processing. We constructed a photonic PSC from electrical PSCs with a novel and simple circuit scheme and electroabsorption modulators (EAMs). By effectively combining electrical multiplexing with optical multiplexing, the photonic PSC can generate a 40-Gbit/s 16-bit optical packet from 16 parallel channels of electrical signals at packet rates of 40 MHz. The photonic PSC has several advantages, including support for asynchronous burst signal input, compactness, and low power consumption. The electrical PSC has also been applied to a label comparator for bypass/drop self-routing of 10-Gbit/s asynchronous optical packets.

1. Introduction

Due to the increasing optical signal bit rates of optical communication systems, it is becoming harder to implement regular signal processing functions on electronic circuits when direct optical-electrical (OE) conversion is used. Photonic serial-to-parallel converters (SPCs) and parallel-to-serial converters (PSCs) are very promising because they provide an interface that enables us to use low-speed but smart silicon electronic circuits, such as a CMOS (complementary metal-oxide-semiconductor) processor, to handle high-speed optical signals. **Figure 1** shows our concept of a photonic packet processor [1] in which a silicon electronic processor is sandwiched between an all-optical SPC and a photonic PSC. The all-optical SPC converts a high-speed optical signal into n parallel slow electrical signals through a low-speed PD array. The n parallel electrical signals are sent to the silicon CMOS processor. Then, after packet processing (label processing, buffering, 3R (reamplification, reshaping, retiming) regeneration, and packet compression/decompression) has been completed, they are output from the processor and converted into a high-speed optical signal by the photonic PSC. We have reported an all-optical SPC [2], [3] that uses an ultrafast surface-reflection optical switch [4]. The SPC can convert an incoming high-speed (40-Gbit/s to 1-Tbit/s) 16-bit optical packet into 16 parallel optical signals.

Parallel-to-serial conversion of ten 10-Gbit/s electrical data streams to one 100-Gbit/s optical signal

† NTT Photonics Laboratories
Atsugi-shi, 243-0198 Japan
E-mail: kiyoto@aecl.ntt.co.jp

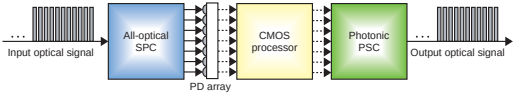

Fig. 1. Conceptual diagram of a photonic packet processor.

has been demonstrated using optical time-domain multiplexing (OTDM) technology [5]. Unfortunately, this scheme requires ten electroabsorption modulators (EAMs) for the ten data streams. Another way to achieve photonic parallel-to-serial conversion is to use high-speed electrical multiplexers that convert, for example, four 10-Gbit/s data streams to a 40-Gbit/s data stream. Such a scheme, however, consumes a lot of power and requires a high-speed optical modulator to convert the electrical data into optical data. Moreover, both schemes are effective only in bit-synchronous systems.

This paper describes a photonic PSC [6] consisting of EAMs and new electrical PSCs [7] with ordinary metal-semiconductor-metal photodetectors (MSM-PDs). An InP-based electrical 4:1 PSC features a novel circuit scheme that markedly improves the response of an ordinary MSM-PD and generates a 10-Gbit/s 4-bit serial electrical signal from 4-ch parallel signals when MSM-PDs are optically triggered. The new circuit scheme provides a highly sensitive compact electrical PSC that operates at low bias voltage, supports burst signal input, and consumes very little power. The effective combination of electrical multiplexing with optical multiplexing enables the photonic PSC to generate a 40-Gbit/s 16-bit optical packet stream from 16-ch parallel electrical data streams. This paper also reports on a label comparator that uses the electrical PSC [7]. Bypass/drop self-routing of 10-Gbit/s optical packets has been successfully demonstrated using the comparator.

2. Electrical PSC

A simple way to build an electrical PSC is to align a linear array of MSM-PDs, spaced at regular intervals, with a transmission line as shown in **Fig. 2**. The MSM-PDs are biased by parallel electrical input signals and optically triggered one by one with appropriate delays. This produces a serial electrical signal containing the same data as the parallel input signal. In this scheme, PIN-type photodetectors cannot be used because they generate an output signal when optically triggered, even when no bias voltage is applied. MSM-PDs are suitable for PSCs because they have no photoresponse in the absence of a bias voltage. However, the impulse response of an ordinary MSM-PD exhibits a long fall time due to its low hole mobility, and this makes it difficult for the PSC to generate a high-speed serial signal with bit separations of less than a few hundred picoseconds.

The fall-time problem has been tackled by fabricating MSM-PDs on low-temperature-grown GaAs [8], [9] and InGaAs/InAlAs multiple quantum wells [10], as well as by making those with a narrow-spacing electrode structure [9], [11]. These approaches, however, sacrifice MSM-PD sensitivity and ease of fabrication for ultrafast electrical pulse generation.

In contrast, our novel and simple circuit scheme reduces the fall time of an ordinary MSM-PD without sacrificing either its sensitivity or ease of fabrication [7]. **Figure 3** shows our proposed circuit and its operating principle. The circuit consists of input resistor R_{in}, hold capacitor C_h, and an MSM-PD. Here, R_d, R_{on}, and V_h are load resistance, on-state resistance of the MSM-PD, and hold voltage, respectively. R_{in} is set much larger than the sum of R_{on} and R_d. An input signal charges up C_h slowly with a time constant of $R_{in}C_h$. When the MSM-PD is optically triggered, charges held in C_h are rapidly discharged, and the bias voltage on the MSM-PD disappears because $R_{in}C_h$ is large enough. Therefore, the response of the circuit is determined by the time constant $C_h(R_{on}+R_d)$ and not affected by the residual holes.

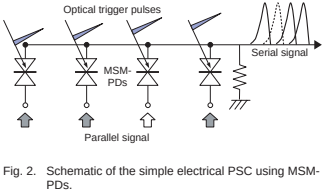

Fig. 2. Schematic of the simple electrical PSC using MSM-PDs.

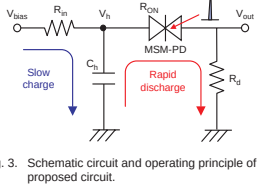

Fig. 3. Schematic circuit and operating principle of the proposed circuit.

The circuit was fabricated using epitaxial layers grown on InP substrate by metal-organic vapor-phase epitaxy. The MSM-PD consists of a 1.5-μm-thick InGaAs photoabsorption layer and an InAlAs Schottky contact layer. The interdigitated MSM-PD has a photosensitive area, line/spacing, and sensitivity of $20 \times 20\ \mu m^2$, 0.75/0.75 μm, and 0.37 A/W, respectively. The input resistor R_{in} was formed using semiconductor layers and the hold capacitor C_h was made using an insulating thin-film SiN_x. For all fabrication processes, including patterning of the interdigitated electrodes of the MSM-PD, conventional photolithography was used.

We measured the impulse response of the circuit and that of a separate directly biased MSM-PD (without C_h or R_{in}) on the same wafer by time-resolved electro-optic sampling with a 1.55-μm incident pulse (FWHM (full width at half maximum) of 600 fs) using an external CdTe probe chip [12]. The separate MSM-PD had the same structure and size as mentioned above. **Figure 4** shows the impulse responses of (a) the separate MSM-PD and (b) the proposed circuit for several optical pump energies. The responses of the circuit have a much shorter fall time than those of the separate MSM-PD. With increasing optical pump energy, the fall time of the MSM-PD becomes longer because of the space charge effect, while that of the circuit becomes shorter because of the smaller CR time constant. For pump energy of 3.6 pJ, it generated a short electrical pulse with FWHM of 3.3 ps.

Figure 5 shows a 4:1 electrical PSC consisting of four of the new circuits. The PSC was fabricated on a wafer with the same epitaxial layers and the MSM-PDs had the same dimensions as the one described above. The MSM-PDs with 250-μm period were aligned alongside a transmission line. Each MSM-PD was connected to a metal-insulator-metal (MIM) capacitor (C_h) of 55 fF and a semiconductor resistor (R_{in}) of 25 kΩ.

Parallel input signals (0–3.0 V) charged up the

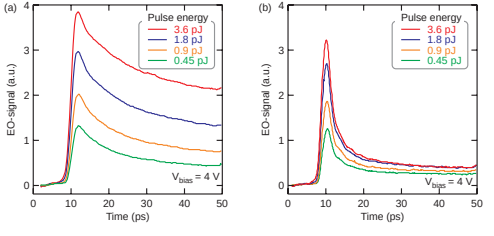

Fig. 4. Measured impulse responses. (a) Separate MSM-PD and (b) the proposed circuit.

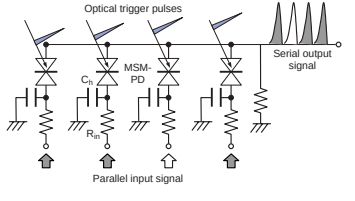

Fig. 5. Schematic circuit of an electrical 4:1 PSC.

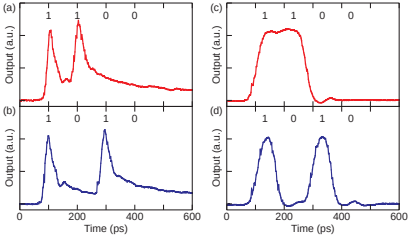

Fig. 6. Output waveforms from (a) the 4:1 PSC for input signal of "1100", (b) the 4:1 PSC for input signal of "1010", (c) the decision IC for input signal of "1100", and (d) the decision IC for input signal of "1010".

capacitors and optical trigger pulses illuminated the four MSM-PDs in order at intervals of 100 ps. **Figures 6(a)** and **(b)** show the waveforms output from the 4:1 PSC for parallel input signals of "1100" and "1010", respectively. The PSC successfully generated 10-Gbit/s 4-bit serial signals corresponding to the parallel input signals. The output signal was reshaped by a decision integrated circuit (IC). The waveforms from the decision IC are shown in **Fig. 6(c)** and **(d)**. Although the output waveforms from the PSC exhibited a slight tail, the decision IC output distinct non-return-to-zero waveforms for the two data patterns. The PSC requires no electrical power supply, only optical trigger pulses, to generate a 10-Gbit/s serial signal.

3. 40-Gbit/s 16-bit photonic PSC

Our photonic PSC is shown in **Fig. 7**. It consists of the four electrical PSCs fabricated on one chip, a surface-emitting planar lightwave circuit (PLC), and four EAMs. An optical pulse from a pulse source is split into three pulses: a trigger pulse for reading data, a trigger pulse for the electrical PSCs, and a source pulse for an output packet. The optical trigger pulse is input to read out data from the CMOS processor and 16-bit data are output in the form of parallel electrical signals. The parallel electrical signals are bundled in groups of four with each group passed to a 4:1 electrical PSC. The trigger pulse for the electrical PSCs

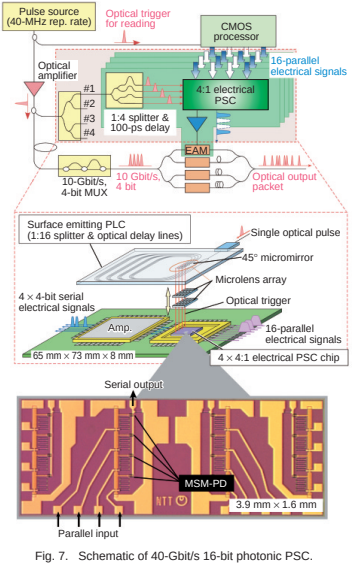

Fig. 7. Schematic of 40-Gbit/s 16-bit photonic PSC.

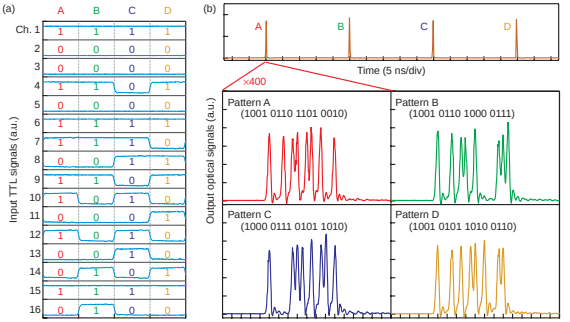

Fig. 8. Measured waveforms of (a) input 16-ch parallel data and (b) output optical packets from the photonic PSC.

is launched into the PLC, which contains a 1:16 splitter, delay lines, and 45° mirrors [13]. The split pulses are emitted from the PLC surface and focused using microlens arrays on each MSM-PD biased by the parallel electrical signals. This configuration provides stable and precise illumination of trigger pulses, and four sets of 10-Gbit/s 4-bit serial electrical signals are generated. The four serial electrical signals are amplified and reshaped and input to the EAMs. The source optical pulse is launched into an optical multiplexer to form a 10-Gbit/s 4-bit pulse train. It is then split into four parts, each of which is modulated by one of the four EAMs. The four 10-Gbit/s 4-bit optical packets are then combined in a bit-interleaved fashion with a bit separation of 25 ps, resulting in generation of a 40-Gbit/s 16-bit optical packet. This type of optical packet generator has several important advantages: it is scalable, owing to the effective combination of electrical and optical multiplexing; it generates ultrafast burst optical packets from much slower parallel electrical data; and it can be driven by a simple, low-cost CMOS logic IC and has low power consumption.

Figure 8(a) shows the input electrical data streams from a 16-ch pulse pattern generator driven at a 40-MHz repetition rate. The 16-ch parallel data alternated among four patterns: A (1001 0110 1101 0010), B (1001 0110 1000 0111), C (1000 0111 0101 1010), and D (1001 0101 1010 0110). Output optical packets from the photonic PSC were measured with a sampling oscilloscope through an OE converter with 30-GHz bandwidth, as shown in **Fig. 8(b)**. The small signals for the "0" states arose because of ringing of the OE converter. The photonic PSC successfully generated 40-Gbit/s 16-bit optical packets corresponding to the four alternating 16-ch parallel data patterns.

4. Label comparator

High-speed optical label processing capability is the key to building large-capacity optical packet-switched networks. The 1×4 self-routing of 40-Gbit/s 16-bit optical-packets has been demonstrated based on bit-by-bit label recognition [14]. Simpler label processing based on all-optical matched-filter-type label-recognition schemes [15], [16] has also been demonstrated. These schemes, however, require control of polarization or wavelength and have difficulty in handling increases in the number of label bits. Here, we describe a simple label comparator using the electrical PSC. This label comparator requires neither polarization nor wavelength control, and it is scalable in terms of the number of label bits.

Figure 9 shows the experimental setup for 1×2 self-routing of 10-Gbit/s 4-bit optical packets using the

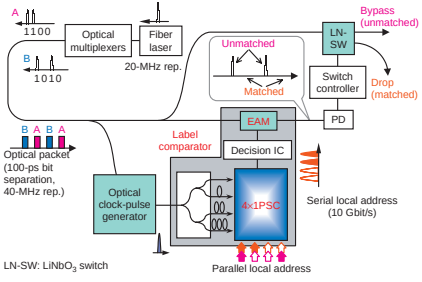

Fig. 9. Experimental setup for bypass/drop self-routing of 10-Gbit/s 4-bit optical packets.

label comparator composed of a 4:1 electrical PSC and an EAM. The optical pulse from a fiber laser with 20-MHz repetition rate was converted into two 4-bit optical signals (A: 1100, B: 1010) with a bit separation of 100 ps using fiber-based optical multiplexers. In this experiment, the 4-bit signal was regarded as an optical packet consisting of a 4-bit label and an empty payload. Packets were split into three and injected into an optical clock pulse generator [17], the EAM and a 1×2 $LiNbO_3$ switch (LN-SW). From each incoming burst optical packet with no preamble, the optical clock pulse generator provides a single optical pulse having a constant pulse width (<10 ps), constant power, and stable timing (<2 ps) when the pulse energy of the first bit is larger than 0.5 pJ. An optical clock pulse synchronized with the incoming packet was launched into the 4:1 PSC. Four-channel parallel electrical signals were input into the PSC as a local address and converted into a 10-Gbit/s serial address signal when the MSM-PDs in the PSC were triggered by the optical clock pulses. The 10-Gbit/s-address signal, after it was reshaped by the decision IC and amplified, drove the EAM, which acted as a logic gate. Here, the EAM gate was set to be normally open and the number of "1" bits in the packet and the local address were identical. The input optical packet was therefore erased only when the optical packet completely matched the local address. Therefore, in the matched case, no signal voltage was applied on the LN-SW and the packet was output from the drop port. In the unmatched case, part of the packet passed through the EAM and was converted into an electrical control signal by a photodetector. The controller then applied a switching voltage to the LN-SW to guide the packet to a bypass port.

Figure 10 shows the input local address and output optical signals from bypass and drop ports. When the local address alternated between "1100" and "1010" with 40-MHz repetition rate, packets A and B matched the local address and were output from the drop port, and no signal was observed at the bypass port (**Fig. 10(a)**). On the other hand, when the local address cycled between "1100" and "1001", packet A was output from the drop port, while packet B was output from the bypass port because it failed to match the local address (**Fig. 10(b)**). The crosstalk to the other port was less than –15 dB, which was determined by the extinction ratio of the LN-SW. These results indicate that the label comparator properly processed the optical 10-Gbit/s 4-bit labels and accurately switched the optical packets.

5. Conclusion

For application in optical packet processors, we have demonstrated a 16:1 photonic parallel-to-serial converter (PSC) that can generate a 40-Gbit/s 16-bit optical packet from 16-ch parallel electrical signals at the packet rate of 40 MHz. Because the photonic PSC uses new electrical PSCs and effectively combines electrical and optical multiplexing, it has many advantages, including support for burst signal input, compactness, low power consumption, scalability in terms of input channel number, and compatibility

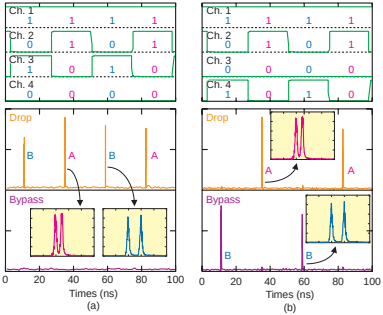

Fig. 10. Waveforms of input local address and output from bypass and drop ports. Insets show magnified waveforms of the output optical packets. (a) Local address cycled between "1100" and "1010". (b) Local address cycled between "1100" and "1001".

with CMOS circuits. This electrical PSC has also been used in a label comparator for bypass/drop switching of 10-Gbit/s asynchronous optical packets.

References

[1] K. Takahata, R. Takahashi, T. Nakahara, H. Takenouchi, and H. Suzuki, "Photonic packet router for 40-Gbit/s 16-bit burst optical packets," Proc. of OFC 2004, TuQ3, Los Angeles, California, U.S.A., Feb. 2004.

[2] R. Takahashi and H. Suzuki, "1-Tbit/s, 16-bit all-optical SPC using a surface-reflection all-optical switch," IEEE Photon. Technol. Lett., Vol. 15, No. 2, pp. 287-289, 2003.

[3] R. Takahashi, T. Yasui, N. Kondo, and H. Suzuki, "40-Gbit/s 16-bit label recognition using planar-lightwave-circuit-based all-optical serial-to-parallel converter," Electron. Lett., Vol. 39, No. 15, pp. 1135-1136, 2003.

[4] R. Takahashi, "Low-temperature-grown surface-reflection all-optical switch (LOTOS)," Optical and Quantum Electronics, Vol. 33, pp. 999-1017, 2001.

[5] J. K. Lucek, A. D. Ellis, D. G. Moodie, D. Pitcher, P. Gunning, and D. Cotter, "100 Gbit/s parallel-to-serial and serial-to-parallel conversion using electroabsorption modulators," Proc. 1998 IEEE/LEOS Summer Topical Meetings, TuB3, Monterey, California, U.S.A., pp. 25-26, July 1998.

[6] H. Takenouchi, K. Takahata, T. Nakahara, R. Takahashi, and H. Suzuki, "40-Gbit/s-to-10-Gbit/s 16-bit burst optical packet generator based on photonic parallel-to-serial conversion," IEICE Trans. Electron., Vol. E87-C, No. 5, pp. 825-827, 2004.

[7] K. Takahata, H. Takenouchi, T. Nakahara, R. Takahashi, and H. Suzuki, "Electrical parallel-to-serial converter using MSM-PDs for optical communication networks," Proceedings of SPIE Photonic West 2003, Vol. 4998, pp. 76-84, Jan. 2003.

[8] R. Urata, R. Takahashi, V. A. Sabnis, D. Miller, and J. S. Harris Jr., "Ultrafast Differential Sample and Hold Using Low-Temperature-Grown GaAs MSM for Photonic A/D Conversion," IEEE Photonics Technol. Lett., Vol. 13, pp. 717-719, 2001.

[9] J.-W. Shi, K. G. Gan, Y. J. Chiu, Y.-H. Chen, C.-K. Sun, Y. J. Yang, and J. E. Bowers, "Metal-semiconductor-metal traveling-wave photodetectors," IEEE Photonics Technol. Lett., Vol. 13, pp. 623-625, 2001.

[10] M. Yoneyama, T. Shibata, E. Sano, Y. Kawamura, R. Takahashi, T. Enoki, T. Nagatsuma, and M. Yaita, "A Differential Photoconductive AND Gate with Be-Doped Low-Temperature-Grown InGaAs-InAlAs MQW MSM-PDs," IEEE J. Quantum Electron., Vol. 33, pp. 1308-1315, 1997.

[11] S. Y. Chou and M. Y. Liu, "Nanoscale tera-hertz metal-semiconductor-metal photodetectors," IEEE J. Quantum Electron., Vol. 28, pp. 2358-2368, 1992.

[12] K. Takahata, R. Takahashi, T. Nakahara, H. Takenouchi, and H. Suzuki, "Ultrashort electrical pulse generation using a normal metal-semiconductor-metal photodetector," Proc. of CLEO Europe 2003, CJ3-2, München, Germany, June 2003.

[13] H. Terui and K. Shutoh, "Novel micromirror for vertical optical path conversion formed in silica-based PLC using wettability control of resin," J. Lightwave Technol., Vol. 16, pp. 1631-1639, 1998.

[14] T. Nakahara, R. Takahashi, H. Takenouchi, K. Takahata, and H. Suzuki, "16-bit programmable label swapping for 40-Gbit/s optical packets," ECOC2003-PD, Th4.3.6, Rimini, Italy, Vol. 6, pp. 70-71, Sep. 2003.

[15] D. Cotter, J. K. Lucek, M. Shabeer, K. Smith, D. C. Rogers, D. Nesset, and P. Gunning, "Self-routing of 100 Gbit/s packets using 6 bit 'keyword' address recognition," Electron. Lett., Vol. 31, pp. 2201-2202, 1995.

[16] O. Wada, H. Harai, W. Chujo, and F. Kubota, "Multi-hop, 40 Gbit/s variable length photonic packet routing based on multi-wavelngth label switching, waveband routing, and label swapping," Tech. Dig. of OFC'02, WG3, Anaheim, California, U.S.A., pp. 216-217, Mar. 2002.

[17] T. Nakahara, R. Takahashi, H. Takenouchi, and H. Suzuki, "Optical Single-Clock-Pulse generator Using a Photoconductive Sample-and-Hold Circuit for Processing Ultrafast Asynchronous Optical Packets," IEEE Photonics Technol. Lett., 14, pp. 1623-1625, 2002.

Kiyoto Takahata
Senior Research Engineer, Advanced Optoelectronics Laboratory, NTT Photonics Laboratories.
He received the B.E. and M.E. degrees in physical engineering from Kyoto University, Kyoto in 1988 and 1990, respectively. In 1990, he joined NTT Opto-electronics (now Photonics) Laboratories, Kanagawa, Japan, where he was initially engaged in research on a wavelength conversion device based on a semiconductor DBR laser. Since 1993 he has been working on the design and evaluation of high-speed monolithically integrated photoreceivers. He is now studying ultrafast optical packet processing based on optoelectronic circuits. He is a member of the Japan Society of Applied Physics (JSAP) and the Institute of Electronics, Information and Communication Engineers of Japan (IEICE).

Hirokazu Takenouchi
Research Engineer, Advanced Opto-electronics Laboratory, NTT Photonics Laboratories.
He received the B.S. and M.S. degrees in pure and applied sciences from the University of Tokyo, Tokyo in 1992 and 1994, respectively. In 1994, he joined the NTT Opto-electronics (now Photonics) Laboratories, Kanagawa, Japan, where he was initially engaged in research on vertical-cavity surface-emitting lasers. Since 1997, has been engaged in the research on ultrafast optical signal processing by spectral filtering. He is now studying ultrafast optical packet processing. He is a member of JSAP and IEICE.

Tatsushi Nakahara
Senior Research Engineer, Advanced Optoelectronics Laboratory, NTT Photonics Laboratories.
He received the B.S. and M.S. degrees in applied physics from the University of Tokyo, Tokyo in 1988 and 1990, respectively. In 1990, he joined NTT Opto-electronics (now Photonics) Laboratories, Kanagawa, Japan, where he was initially engaged in research on smart pixels integrating electronic logic circuits with quantum-well modulators or vertical-cavity surface-emitting lasers. Since 1999, he has been engaged in research on high-speed optical packet processing and switching based on optoelectronic circuits. He is a member of the Optical Society of America and JSAP.

Ryo Takahashi
Senior Research Engineer, Advanced Optoelectronics Laboratory, NTT Photonics Laboratories.
He received the B.E., M.E., and D.E. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1987, 1989, and 1992, respectively. In 1992, he joined NTT Opto-electronics Laboratories, Kanagawa, Japan. From 1998 to 1999, he was a visiting scholar at the Ginzton Laboratory, Stanford University, Stanford, CA. Currently, he is engaged in R&D of ultrafast all-optical devices and optical packet processing technologies for optical packet-switched networks. He is a member of JSAP and IEICE.