Ultrafast Multifunctional CMOS LSI with 12.5-Gbit/s Transceiver

Tomoaki Kawamura† *and Yusuke Ohtomo*

Abstract

We have developed ultrafast CMOS LSI (complementary metal oxide semiconductor large-scale integration) technology that can be used to produce ultrafast transmitting/receiving circuits (including signal receiver circuits and logic circuits) that have comfortable operating margins even at speeds as high as 12.5 Gbit/s. This technology can be used to implement ultrafast multifunctional LSIs that are needed for the efficient processing of high-volume communications. We have used it to fabricate an ultrafast multifunctional CMOS LSI in which the functions necessary for testing and evaluating LSIs that transmit and receive signals at 10 Gbit/s or above are integrated into a single chip.

1. Importance of ultrafast multifunctional LSIs

To handle Internet communications efficiently, carriers are introducing networks that perform 10-Gbit/s wideband communication across Ethernet links, which are widely used in local area networks. Research on providing more services by using wavelength division multiplexing (WDM) to allocate wavelengths to different users or services is also progressing. In the devices used to implement these networks, it is essential that ports capable of transmitting and receiving signals at 10 Gbit/s or more are implemented with multiple channels for WDM applications. The key issue to consider when constructing such a network is how to provide these ultrafast multi-channel ports using compact low-cost components. There is also a need for technology that can implement ultrafast multifunctional LSIs with a favorable cost/performance ratio that incorporate large-scale logic functions such as network administration, billing, and the provision of diverse services.

If CMOS LSIs capable of transmitting and receiving 10-Gbit/s signals can be made, then they can be used to implement ultrafast multifunctional LSIs. However, with conventional technology, it has been impossible to make them transmit and receive 10-Gbit/s signals with a speed margin of at least 25%. At NTT Microsystem Integration Laboratories, we have developed ultrafast CMOS LSI (complementary metal oxide semiconductor large-scale integration) technology that can achieve transmission and reception at 12.5 Gbit/s in CMOS LSIs with large operating margins by using an ultrafast signal receiver circuit with a new parallel architecture and ultrafast logic circuits that use on-chip inductors and on-chip capacitors.

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2. Example of ultrafast multifunctional LSI configuration

As an example of an ultrafast multifunctional LSI, **Fig. 1** compares the configuration of a conventional device with that of an ultrafast multifunctional LSI that incorporates signal transceiver units for a 10-Gbit/s communication device. As Fig. 1(a) shows, the communication device for 10-Gigabit Ethernet (10GbE) communications achieves a speed of 10 Gbit/s by using multiple LSIs, including ultrafast LSIs that transmit and receive ≥10-Gbit/s signals and an LSI for processing the encoding and decoding. Here, the speed at which optical signals are transmitted and received is 3–25% greater than the 10-Gbit/s signal speed before encoding. If an ultrafast multifunctional LSI can be implemented in which the functions of these multiple LSIs are integrated into a single chip, as shown in Fig. 1(b), then it will be possible to greatly improve the cost/performance ratio of

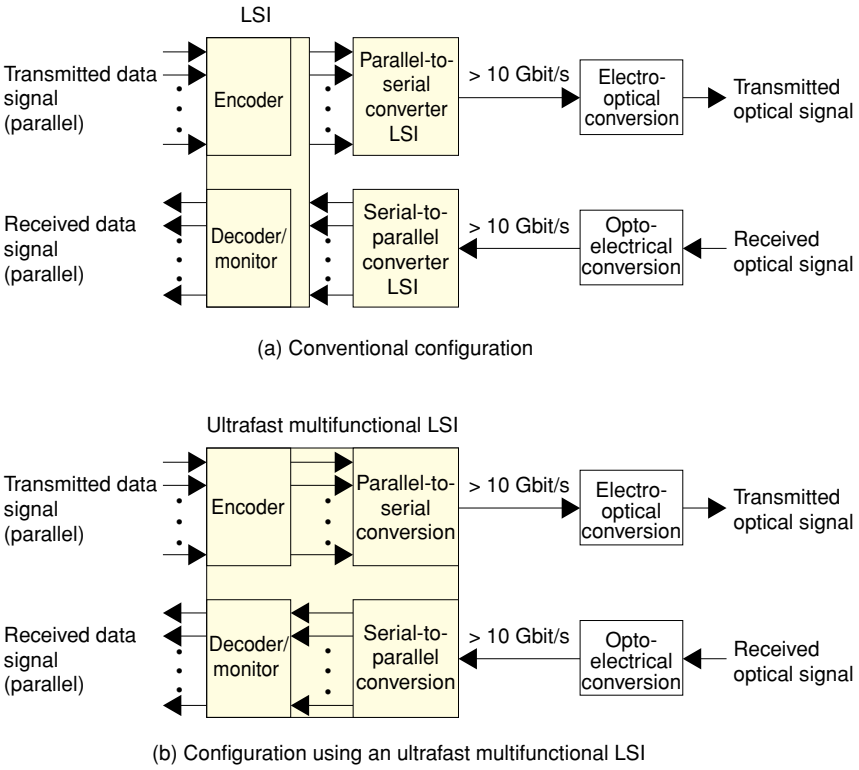


Fig. 1. Configuration of signal transceiver units for 10-Gbit/s communication devices.

the equipment for 10-Gbit/s communication.

This functional integration also makes it possible to, for example, incorporate all the functions of four ultrafast multifunctional LSIs, as shown in Fig. 1(b), into a single LSI. The development of an LSI like this would have a major impact on the capacity and cost of WDM equipment capable of carrying multi-channel (e.g., 8-channel) 10GbE signals through a single optical fiber.

3. Ultrafast CMOS LSI technology

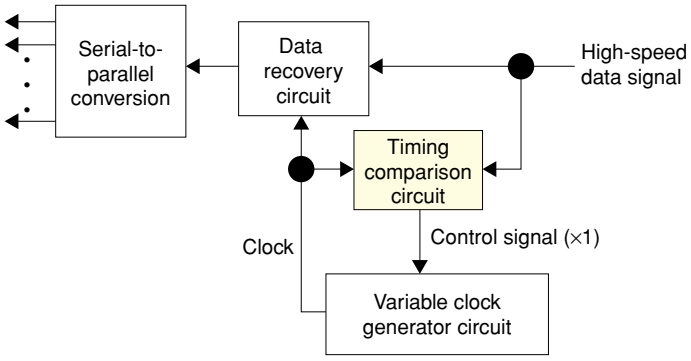
Ultrafast LSIs for transmitting and receiving 10-Gbit/s signals have generally been made using compound semiconductor LSIs and SiGe LSIs. However, these LSIs have been too costly for implementing complex functions such as the encoding processes shown in Fig. 1. Instead, less-expensive CMOS LSIs are generally used to implement these complex functions. This section describes our ultrafast CMOS LSI technology that can transmit and receive at 12.5 Gbit/s in CMOS LSIs with large operating margins.

3.1 Ultrafast signal receiver circuit

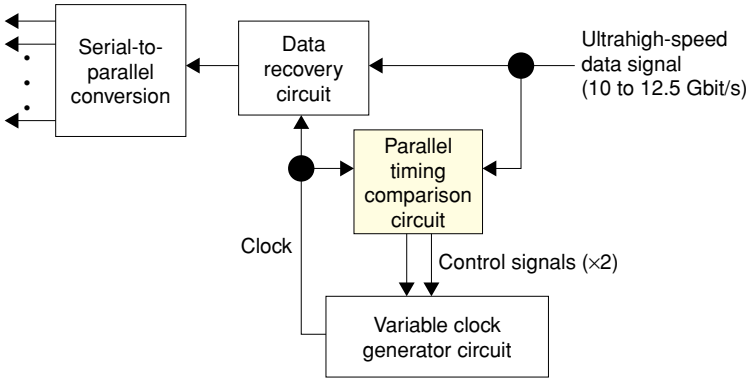
A major issue in transmitting and receiving ≥10-Gbit/s signals with large operating margins is making circuits to receive these signals. We have developed a new parallel architecture that increases the speed of the receiver circuits. **Figure 2** compares the configuration of an ultrafast signal receiver circuit using this parallel architecture with that of a conventional high-speed signal receiver circuit. This receiver circuit corresponds to the serial/parallel converter unit shown in Fig. 1(b). In the conventional circuit (Fig. 2(a)), the timing of the input data signal is compared with an internally generated clock by a timing comparison circuit, and the variable clock generator circuit is controlled with a single control signal. This control signal must be output at a speed of at least twice that of the input data, so the operating speed of the receiver circuit as a whole is limited by the performance of the timing comparison circuit. In the parallel architecture, this problem is addressed by using a parallel timing comparison circuit that compares a single bit of data in each time period and outputs two control signals at half the speed of the conventional configuration. This relaxes the operating speed constraints on the timing comparison circuit, enabling us to receive data signals at 10–12.5 Gbit/s.

3.2 Ultrafast logic circuit

With conventional high-speed logic circuits, it has been difficult to achieve operating speeds over 10



(a) Configuration of a conventional high-speed signal receiver circuit



(b) Configuration of an ultrafast signal receiver circuit

Fig. 2. Signal receiver circuit configurations.

Gbit/s because of the relatively slow response speed of MOS transistors, but we have developed ultrafast logic circuits that use on-chip inductors and on-chip capacitors and can operate at over 10 Gbit/s. **Figure 3** shows the configurations of a conventional high-speed logic circuit and our ultrafast logic circuit. On-chip inductors L1 and L2 (Fig. 3(b)) are integrated by forming spiral-shaped lines in the LSI. They raise the operating speed of the logic circuit by using the effect whereby inductors convert current variations into voltage variations. On-chip capacitors C1 and C2 and on-chip resistors R1 and R2 in Fig. 3(b) are used to replace transistor Q3 in Fig. 3(a) and to merge current-switching and current-control functions into transistors Q1 and Q2, as shown in Fig. 3(b). In the conventional logic circuit (Fig. 3(a)), transistors Q1 and Q2 are used for current switching and Q3 is used for current control. Removing Q3 increases the response speeds of Q1 and Q2 in Fig. 3(b) compared with Q1 and Q2 in Fig. 3(a) under the same operating voltage (VDD-VSS) and current.

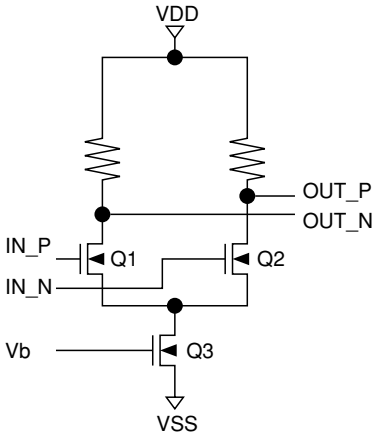
In simulations with the same operating voltage (VDD-VSS) and current, the ultrafast logic circuits having on-chip inductors and capacitors in Fig. 3(b) achieved operating speeds ranging from 1.5 to 2 times faster than those of the conventional high-speed logic circuits in Fig. 3(a).

4. Example of ultrafast multifunctional LSI implementation

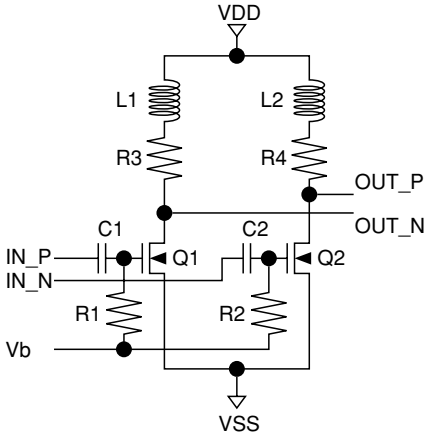
Figure 4 shows the configuration and a photograph of an ultrafast multifunctional LSI implemented as a CMOS LSI that can transmit and receive ≥10-Gbit/s signals and perform complex functions. This LSI integrates the functions necessary for testing and evaluating LSIs that transmit and receive ≥10-Gbit/s signals into a single CMOS LSI. In addition to an ultrafast signal receiver circuit, it incorporates a parallel-to-serial converter circuit for transmitting ≥10-Gbit/s signals. We have confirmed that this LSI operates correctly at speeds of 10–12.5 Gbit/s. This LSI enables us to test and evaluate LSIs for 10GbE.

5. Future work

By applying this technology to optical access LSIs, we aim to improve the cost/performance ratio of equipment used for broadband services.

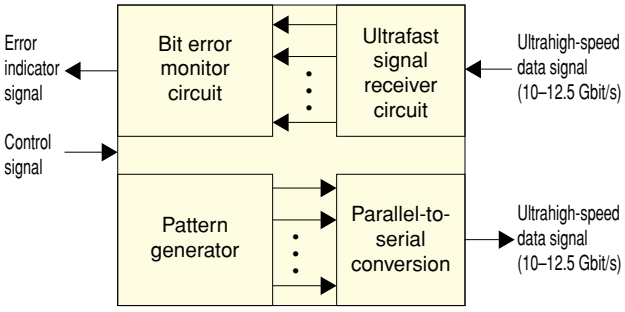


(a) Conventional high-speed logic circuit

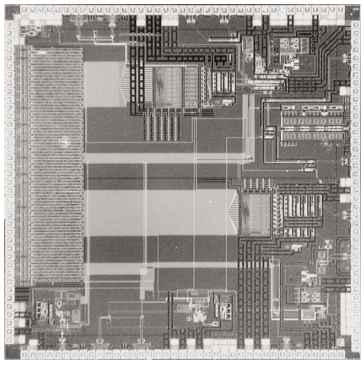


(b) Ultrafast logic circuit with on-chip inductors and on-chip capacitors

Fig. 3. Logic circuits.



(a) Configuration



Chip size: 5 mm × 5 mm

(b) Chip photograph

Fig. 4. Ultrafast multifunctional CMOS LSI.

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He received the B.E. and M.E. degrees in electrical engineering from Tohoku University, Sendai, Miyagi in 1988 and 1990, respectively. Since joining NTT in 1990, he has been engaged in R&D of high-speed Si bipolar integrated circuits and high-speed switching systems. He is currently researching and developing ultrahigh-speed integrated circuits using low-cost CMOS devices. He received the best of conference award from the 48th IEEE Electronic Components and Technology Conference in 1999. He is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) and the Japan Society of Applied Physics.

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