System LSIs for Digital Broadcasting Applications

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Abstract

This article describes two MPEG-2 codec LSIs (large-scale integrated circuits). VASA is a professional single-chip MPEG-2 422P@HL codec with a multichip configuration for large-scale processing beyond the HDTV (high-definition television) level. ISIL is a consumer/prosumer single-chip full-duplex MPEG-2 codec LSI with HDV (high-definition video) compliance for embedding in mobile and small codec systems. Demonstrations of several digital broadcasting applications are also reported. The VASA and ISIL implementations provide compact, low-power, reliable infrastructure and peripheral systems for practical terrestrial digital broadcasting.

1. Motivation for MPEG-2 chip development

Recent progress in video and audio compression technology has made it possible to provide a much greater quantity and range of digital multimedia. The MPEG-2 standard [1] has emerged as a method for effectively compressing video and audio with high quality. In particular, this standard is currently seeing extensive worldwide use in many transmission and storage applications, such as digital satellite broadcasting, digital terrestrial broadcasting, digital cable television, video conferencing, video-on-demand, and DVD and CD-ROM storage media. In particular, the advent of high-quality HDTV (high-definition television) terrestrial digital broadcasting in Japan at the end of 2003 required high-quality, compact, low-power, reliable MPEG-2 HDTV codecs for infrastructure and peripheral systems of practical terrestrial broadcasting.

We have developed several MPEG-2 codec chips and systems during the last ten years, as shown in **Fig. 1**. In 1995, we presented a two-chip MPEG-2 SP@ML[*1] video encoder chip set [2] and introduced the MPEG-2 PCI board that we had developed earlier. In 1998, we presented a single-chip MPEG-2 MP@ML video encoder chip (called SuperENC [3]) with an HDTV extension. This chip made possible our small "1U-half-rack-sized portable HDTV encoder for professional use" [4] and the small "encoding PC card for notebook PCs" [5]. In 2002, we announced two MPEG-2 codec LSIs (large-scale integrated circuits). One was VASA, the world's first single-chip MPEG-2 HDTV codec LSI [6] for professional contribution transmission (explained in sections 2.1 and 3.1) in Japanese digital terrestrial broadcasting. The other was ISIL [7], [8], a consumer/prosumer[*2] single-chip full-duplex MPEG-2 codec LSI with HDV (high-definition video) compliance for embedding in mobile and small codec systems. Using these chips, we have also developed several compact, low-power, reliable infrastructure and peripheral systems for practical terrestrial digital broadcasting.

2. Architectures of VASA and ISIL

2.1 Target applications

The target applications of VASA and ISIL are shown in **Fig. 2**. VASA is for professional use and is

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*1 SP@ML: An MPEG-2 profile. This stands for simple profile (SP) at the main level (ML). For more details, see http://en.wikipedia.org/wiki/MPEG-2 for example, which gives resolutions and frame rates etc. Other profiles mentioned in this article are MP@ML (main profile at the main level) and 422P@HL (4:2:2 profile at the high level).

*2 Prosumer: a word coined by combining professional and consumer. It is describes high-end consumer equipment.

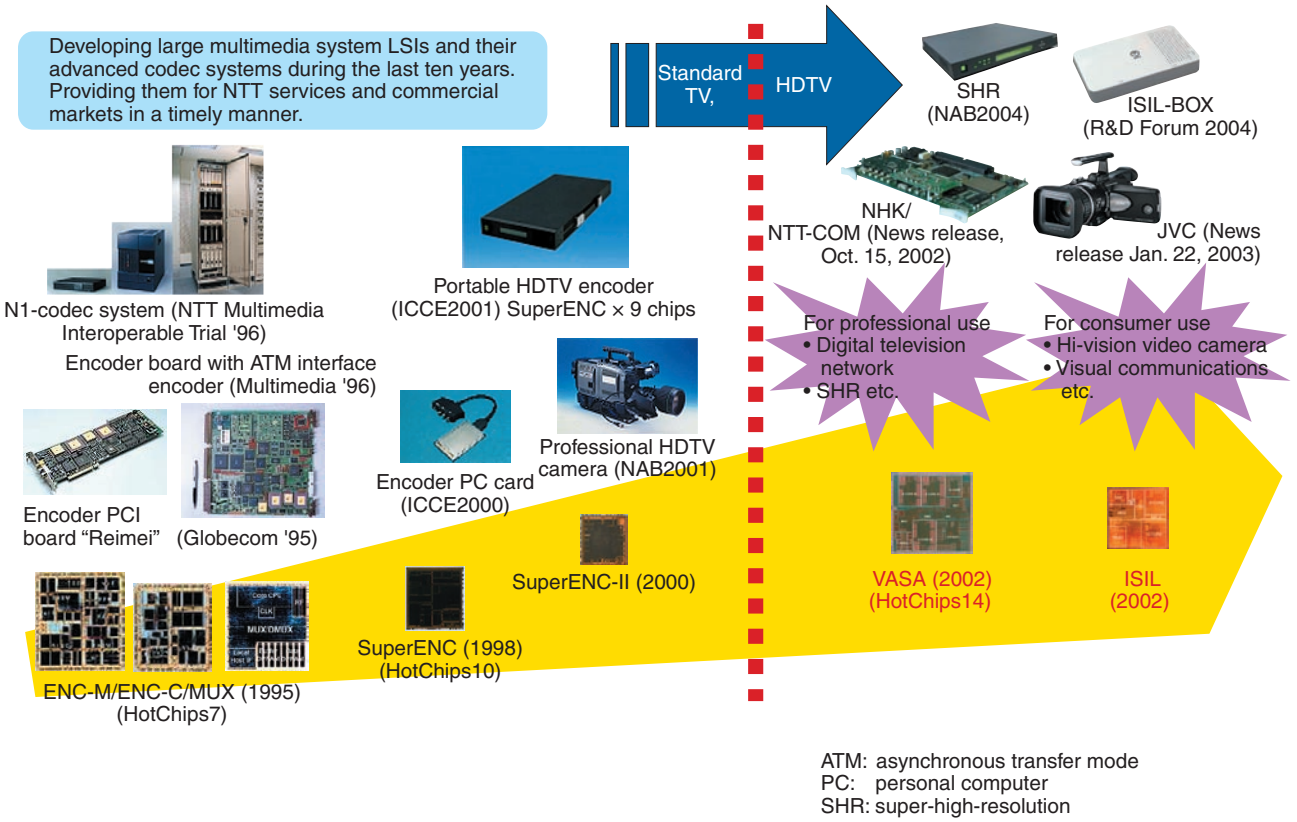


Fig. 1. History of MPEG-2 chips in NTT.

used for contribution transmission (original material transmission before authoring) (explained in section 3.1)), while ISIL is for consumers and prosumers and is used for low-power, inexpensive information appliances. The figure shows resolution and frame rate as a measure of codec performance. VASA covers the entire figure but mainly supports 1080i (1080 lines of vertical resolution with interlaced scanning) for half-duplex processing (either encoding or decoding) in a single chip and super-high-definition beyond HDTV in multiple chips. In contrast, ISIL covers under-720/30p (30p: 30 frames per second with progressive scanning) encoding and mainly supports full-duplex 480i/480p; it supports 1080i only for decoding.

2.2 VASA hardware

VASA consists of three encoding cores (E-COREs), a decoding core (D-CORE), a multiplexer/demultiplexer core (MDX), a video interface/display (VIF/DISP), a watermark (WMK) module, a top-chip RISC (reduced instruction set computer) processor (TRISC), and several dedicated application-specific hardware modules with multichip data transfer (MDT) and a memory interface (MIF) for a hierarchical flexible communication scheme for high-performance data transfer [9]. VASA implements MPEG-2 video and system codecs with generic audio codec interfaces. It provides not only an MPEG-2 422P@HL codec but also large-scale processing beyond the HDTV level for digital cinema and multiview/multi-angle live TV applications when a multichip configuration is used.

VASA's hierarchical flexible communication for the control and data of parallel encoding is based on macroblock pipelined schemes in each parallel encoding core and between cores with a two-level memory hierarchy for the intra- and inter-cores. All application-specific hardware modules and cores dedicated to the MPEG-2 implementation are connected to both a hierarchical CPU bus for small amounts of control data and to a hierarchical system bus for huge amounts of picture data. The flexible communication in a chip is performed by the TRISC and MIF, while the flexible communication in a core is performed by video RISCs (VRISCs) and data interfaces (DIFs). The MIF controls the external

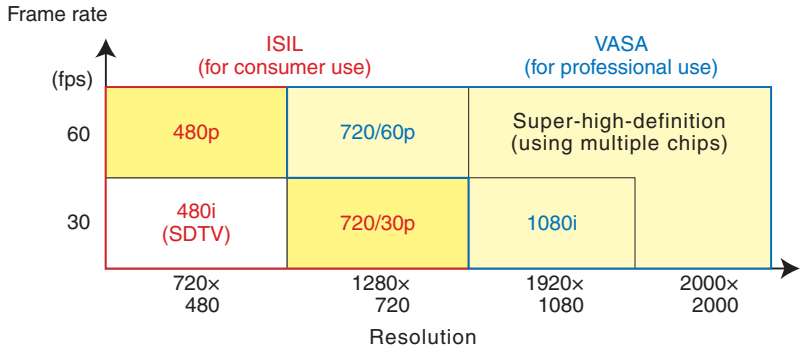
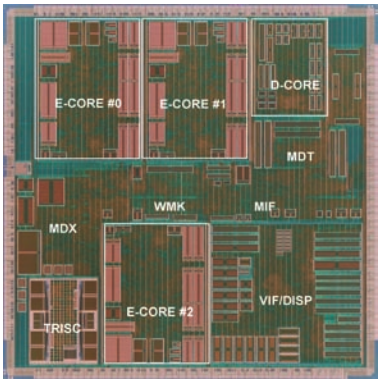
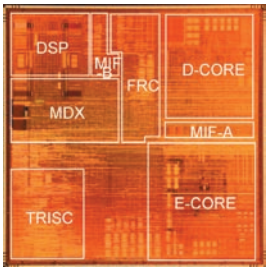


Fig. 2. Target applications of VASA and ISIL.





Process technology	0.13-μm 8-level metal CMOS
Number of transistors	61.4 million transistors
Clock frequency	200 MHz
Supply voltage	Core: 1.5 V, I/O: 3.3 V/DDR: 2.5V
Power consumption	5.0 W (at 1080I 422P@HL)
Package	1008-pin FCBGA (35 mm × 35 mm)

Process technology	0.13-μm 7-level metal CMOS
Number of transistors	30.7 million transistors
Clock frequency	81/108/144 MHz
Supply voltage	Core: 1.5 V, I/O: 3.3 V
Power consumption	1.1 W (at 720/30P encoding)
Package	457-pin BGA (17 mm × 17 mm)

FC-BGA: flip-chip ball grid array

Fig. 3. Microphotograph and physical features of VASA (left) and ISIL (right).

DDR-SDRAMs (double data rate synchronous dynamic random access memories) in order to minimize their input/output rate. The inter-chip data transfer through the MDT enables the VASA chips to use the data on other VASA chips for a multichip configuration.

2.3 VASA software

The VASA software consists of three layers: the hardware layer, the hardware control layer, and the function layer [9]. The hardware control layer is TRISC and VRISC software for controlling the VASA hardware, while the function layer is TRISC software for handling MPEG-2 common basic functions and customized functions for each user. Communication between the hardware layer and the hardware control layer is accomplished via the hardware/software interface in the VASA hardware. Communication between the hardware control layer and the function layer is accomplished via the common function interface in TRISC. Communication between MPEG-2 common basic functions and the user customized functions is carried out via the customized function interface. This software hierarchy not only completely frees users from the tedious task of controlling VASA hardware using the low-level hardware/software interface and the difficulty of handling MPEG-2 common basic functions, but also provides a simple programming interface as a custom function.

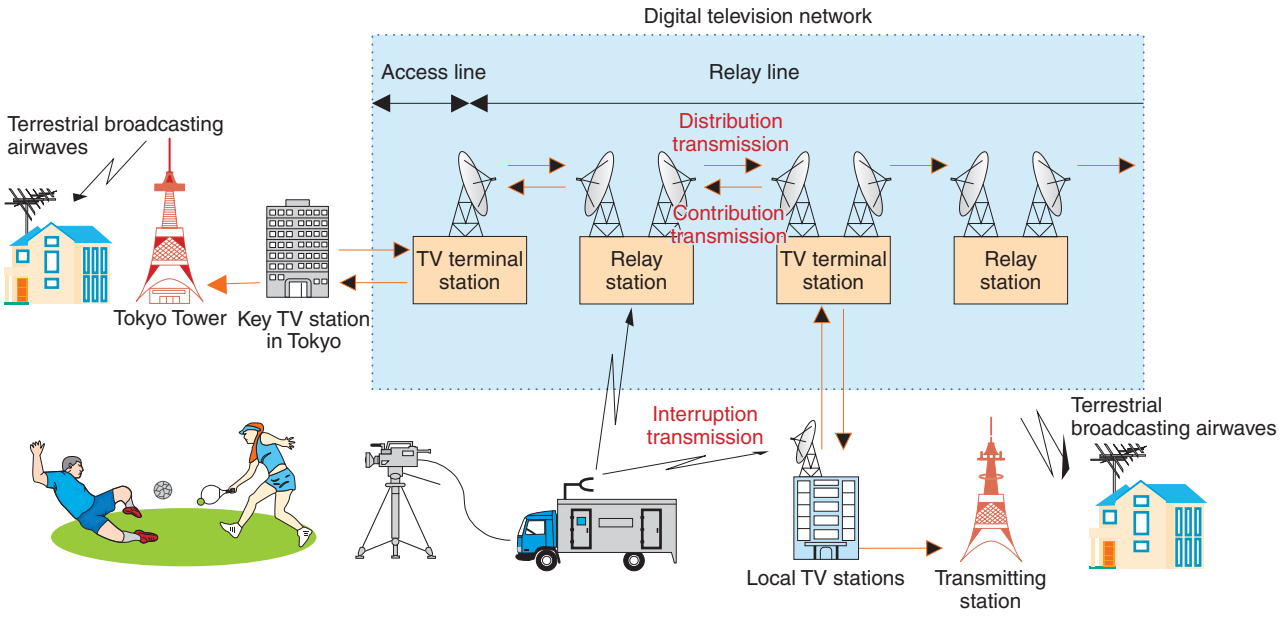


Fig. 4. TV broadcasting mechanism and TV network service in Japan [10].

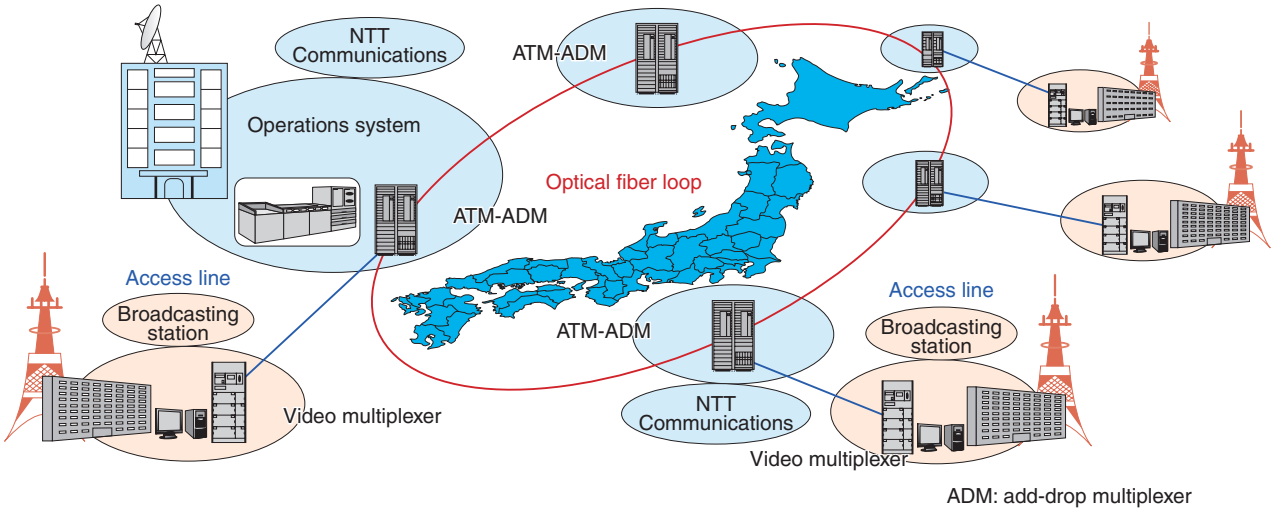


Fig. 5. Digital terrestrial broadcasting network [10].

2.4 Chip characteristics of VASA and ISIL

The physical features of the fabricated VASA and ISIL LSIs are shown in **Fig. 3**. VASA integrates 61.4 million transistors in a 14.0 mm × 14.0 mm chip using 0.13-µm 8-level metal CMOS (complementary metal oxide semiconductor) technology. ISIL integrates 30.7 million transistors in a 10.0 mm × 10.0 mm chip using 0.13-µm 7-level metal CMOS technology. Microphotographs of these LSIs are also shown in Fig. 3. As can be seen, VASA integrates a TRISC, three E-COREs, a D-CORE, an MDX, a VIF/DISP, a WMK, an MDT, and an MIF, while ISIL integrates a TRISC, a single E-CORE, a D-CORE, an MDX, a frame rate converter (FRC), a digital signal processor (DSP), and two MIFs. All the logic circuits on these chips were constructed using only standard cells in order to shorten the design time. Hard macros were not used except for the memories and the TRISC.

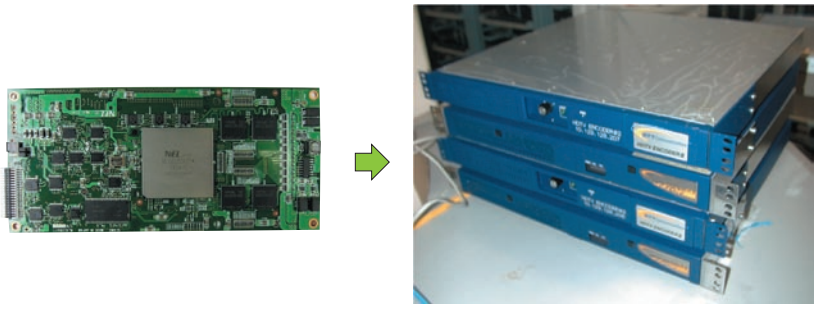


Fig. 6. HDTV codec system for contribution transmission of digital terrestrial broadcasting [10].

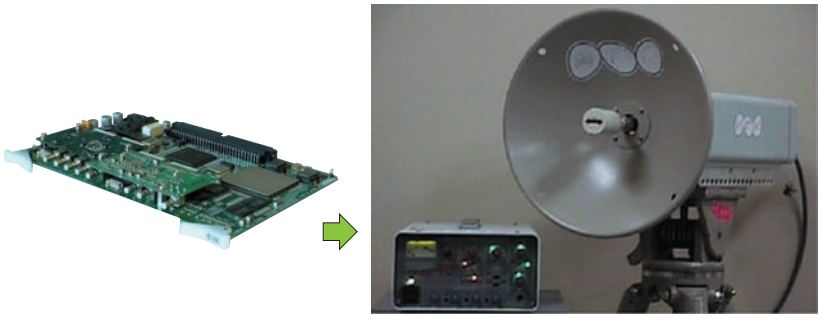


Fig. 7. Very compact HDTV codec system for digital field pickup unit [11].

3. Digital terrestrial broadcasting and several application systems

3.1 Broadcasting mechanism and digital television network in Japan

The television broadcasting mechanism and the television network system [10] in Japan are shown in **Fig. 4**. The typical ways of transmitting television broadcasting are (1) contribution transmission, (2) interruption transmission, and (3) final distribution transmission. Here, contribution means material before authoring. This is visual contents generated at the key TV station and the local TV stations. Interruption transmission means a temporarily setup contribution. This is visual contents generated outside the stations (such as at live events) using an outside broadcast van. Both contribution and interruption are visual contents before authoring, so the bitrates used are higher than those used for distribution. Distribution means the final-output contents for end-users after authoring; it uses a lower bitrate.

As shown in **Fig. 5**, the digital television network [10] offered by NTT Communications (NTT-COM) in Japan consists of an optical fiber loop line covering the whole country, access lines between edge stations (NTT-COM buildings) and broadcast stations, and an operations center (NTT-COM) that controls the network operations of routing traffic and sharing lines. The digital television network is based on a highly reliable ATM (asynchronous transfer mode) network with a redundant and fault tolerant design for a seamless error-free environment.

3.2 High-end codec systems for broadcasting infrastructure

(1) Contribution transmission system

The VASA module (15.8 cm × 7.2 cm), which contains one VASA LSI and four DDR-SDRAMs, and NTT-COM's contribution transmission codec systems [10] that use this VASA module for the digital television network are shown in **Fig. 6**. This codec system implements an MPEG-2 422P@HL codec for contribution transmission with ATM transmission capability in a "1U-full-rack-sized space" thanks to VASA's compact, low-power, and reliable design. This codec system also provides flexible transcoding capability for changing the bitrate during runtime from the high-bitrate short-GOP for contribution to the low-bitrate long-GOP for distribution (GOP: group of pictures). A large number of these high-end MPEG-2 codec systems have already been put into practical operation in the digital television network

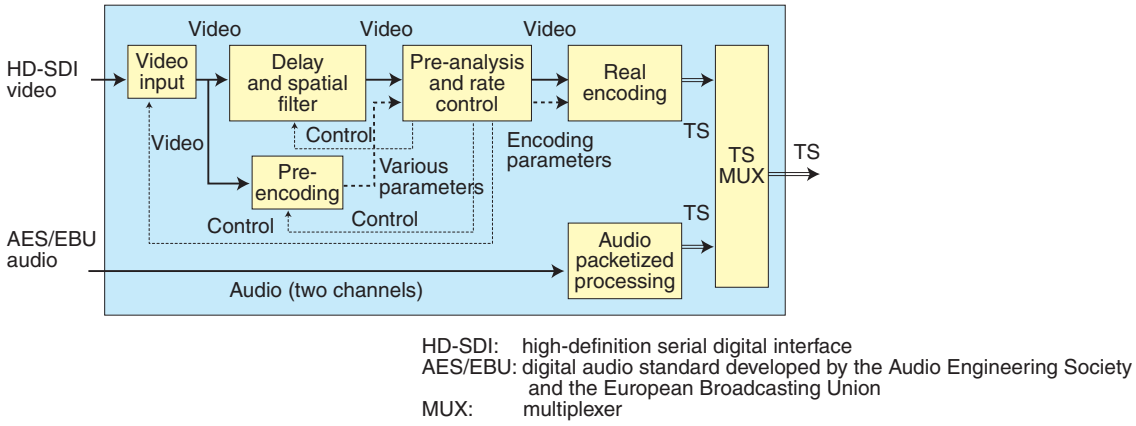


Fig. 8. HDTV encoder system that outputs a high-compression transport stream for digital terrestrial broadcasting [12].

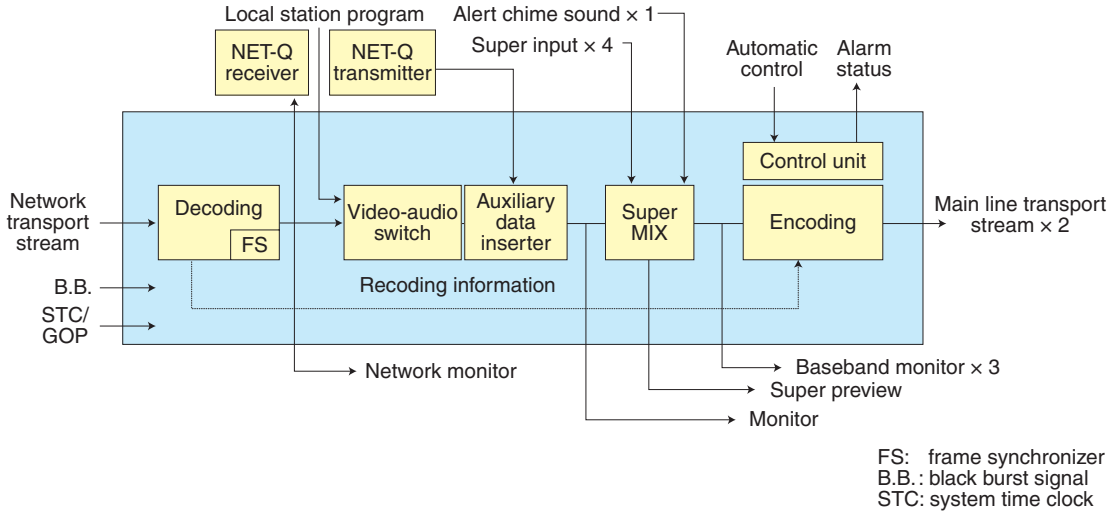


Fig. 9. Seamless TS-switcher for digital terrestrial broadcasting [13].

for Japanese digital terrestrial broadcasting, which started in December 2003.

(2) Interruption transmission system

Using the VASA module, NHK and NTT-COM jointly produced the world's smallest MPEG-2 HDTV codec module, which contains one VASA and a digital field pickup unit [11], which is a portable microwave link for interruption transmission, as shown in **Fig. 7**. This codec system implements an MPEG-2 422P@HL codec for interruption transmission capability in a post-card-sized area. Thanks to VASA, the size and power consumption were drastically reduced to one tenth of previous implementations. This compact codec system will accelerate the portability of HDTV content creation and circulation. A large number of these compact high-end MPEG-2 codec systems have also been in practical operation in the digital television network for Japanese digital terrestrial broadcasting since December 2003.

(3) Distribution transmission system

For contribution transmission, it is important to provide high-quality, low-delay transmission with a high bitrate, which is implemented as simple one-pass encoding. On the other hand, distribution transmission can use a lower bitrate (higher compression ratio) and still maintain end-user quality. VASA is used not only in contribution transmission for simple one-pass encoding, but also in distribution transmission for advanced and more complicated two-pass (or tandem) encoding using recoding information.

The architecture of a high-compression two-pass (tandem) transport stream (TS) output encoder system [12] with VASA for distribution transmission is shown in **Fig. 8**. This encoder system performs real-

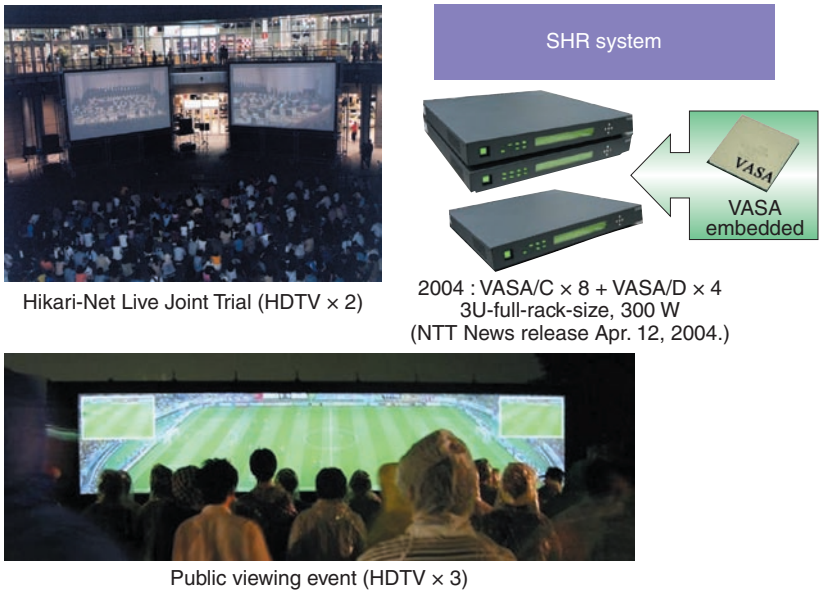


Fig. 10. Future super-high-resolution (SHR) codec system.

time encoding in two passes: first, recoding (previous encoding) information is extracted by pre-analysis encoding; then, real encoding is performed using this recoding information. As a result, a higher compression ratio is achieved. Another advanced encoder, called the TS-switcher (**Fig. 9**) [13], combines transcoding and tandem encoding for seamless blending of the transport stream from the key station and the transport stream from a local station using recoding information. These advanced high-end VASA-based encoder systems have also been used in practical operations by NHK and many commercial broadcasters in the digital television network for Japanese digital terrestrial broadcasting since December 2003.

(4) Super-high-resolution future codec system beyond HDTV-level

Multichip configurations of VASA make it easy to implement future high-quality, high-resolution visual applications beyond the HDTV-level, such as super-high-resolution (SHR) TV (future TV) or digital cinema and/or multiview and multiangle live TV (for sporting or music events). The "1U-full-rack sized" SHR codec system [14] with VASA, which can handle 4000 × 2000 pixels (termed 4K), far exceeding the HDTV-level of 1920 × 1080, is shown in **Fig. 10**. The SHR picture is split into four HDTV images and allocated to several 422P@HL encoders including the VASA chip. After parallel encoding on the VASA multichip configuration, a transport stream of the original SHR picture is output from the bottom of the VASA chip. The left figure in Fig. 10 shows Hikari Net Live: the Saito-Kinen orchestra (two HDTV images) and the bottom figure in Fig. 10 shows a public viewing (three HDTV images). Live music and sports events like these in the SHR TV format will become a popular form of digital multimedia entertainment in the near future.

3.3 Peripheral codec systems for broadcasting infrastructure

The advent of compact consumer/prosumer HDTV video cameras [15] with HDV compliance and embedded small modules [16] is accelerating changes in digital TV content creation and circulation. These days, it is necessary to provide more attractive and dynamic images. The many ISIL-embedded mobile systems, wireless cameras, and module systems have recently made possible a lot of popular and attractive digital TV visual contents and outdoor scenes such as car and yacht races; soccer, baseball, and golf games; orchestral and operatic music events; and athletics events such as the recent Athens Olympic Games.

4. Conclusion and future work

As system LSIs for digital terrestrial broadcasting applications, VASA and ISIL are at the heart of several MPEG-2 professional codec systems used by NTT-COM in the digital television network infra-

structure and by NHK and many other commercial broadcasters for indoor and outdoor use. They have become de facto standards for professional MPEG-2 codec LSIs.

The next-generation advanced video compression standard, called H.264/AVC, is expected to replace MPEG-2 soon. It will offer a higher compression ratio, more than twice that of MPEG-2. We have also been preparing for the H.264 age and have developed a professional H.264 codec chip-set (called SARA [17]) for the high-quality HDTV broadcast infrastructure and SARA-based high-end flexible codec systems that are compact, low-power, reliable, and economical. In the near future, we will implement various actual visual communication services via the IP-based next-generation network, such as IPTV, video-on-demand, and IP re-transmission of digital terrestrial broadcasting airwaves. Through these services, we will contribute to the acceleration and diffusion of the future digital visual society.

References

[1] ISO/IEC13818-1/2/3 International Standard: Information Technology, 1994.

[2] T. Kondo, K. Suguri, M. Ikeda, T. Abe, H. Matsuda, T. Okubo, K. Ogura, Y. Tashiro, N. Ono, T. Minami, R. Kusaba, T. Ikenaga, N. Shibata, R. Kasai, K. Otsu, F. Nakagawa, and Y. Sato, "Two-chip MPEG-2 video encoder," IEEE Micro, Vol. 16, No. 2, pp. 51–58, 1996.

[3] M. Ikeda, T. Kondo, K. Nitta, K. Suguri, T. Yoshitome, T. Minami, J. Naganuma, and T. Ogura, "An MPEG-2 video encoder LSI with scalability for HDTV based on three-layer cooperative architecture," Proc. of Design, Automation and Test in Europe Conference and Exhibition 1999, pp. 44–50, 1999.

[4] T. Yoshitome, K. Nakamura, K. Nitta, M. Ikeda, and M. Endo, "Development of an HDTV MPEG-2 encoder based on multiple enhanced SDTV encoding LSIs," ICCE2001, Los Angeles, pp. 160–161, 2001.

[5] M. Endo, J. Naganuma, Y. Nagajima, and T. Ogura, "An MPEG-2 encoding PC card system for real-time mobile applications," ICCE2000, Sydney, pp. 242–243, 2000.

[6] H. Iwasaki, J. Naganuma, K. Nitta, K. Nakamura, T. Yoshitome, M. Ogura, Y. Nakajima, Y. Tashiro, T. Onishi, M. Ikeda, and M. Endo, "Single-Chip MPEG-2 422P@HL CODEC LSI with Multi-Chip Configuration for Large Scale Processing beyond HDTV Level," Proc. of Proc. of Design, Automation and Test in Europe Conference and Exhibition, 2003, Vol. 2, p. 20002, 2003.

[7] H. Iwasaki, J. Naganuma, Y. Nakajima, Y. Yashiro, K. Nakamura, T. Yoshitome, T. Onishi, M. Ikeda, T. Izuoka, and M. Endo, "A 1.1W single-chip MPEG-2 HDTV codec LSI for embedding in consumer-oriented mobile codec systems," Proc. of CICC2003, San Jose, pp. 177–180, 2003.

[8] NTT Develops High-quality MPEG-2 Codec LSI for Embedding in Consumer-oriented Interactive Video Communication Systems, NTT Technical Review, Vol. 1, No. 1, pp. 97–98, 2003.

[9] J. Naganuma, H. Iwasaki, K. Nitta, K. Nakamura, T. Yoshitome, M. Ogura, Y. Nakajima, Y. Tashiro, T. Onishi, M. Ikeda, M. Endo, and Y. Yashima, "Architecture of Single-chip MPEG-2 HDTV codec LSI—VASA," NTT Technical Journal, Vol. 15, No. 9, pp. 12–15, 2003 (in Japanese).

[10] "Digital TV Transmission Network for Digital Broadcasting," Raisers, Vol. 50, No. 8, pp. 21–25, 2002 (in Japanese).

[11] Y. Nishida and Y. Ito, "Development of Hi-vision CODEC Embedded in Field Pickup Unit (FPU)," Broadcasting Technologies, No. 6, pp. 68–73, 2003 (in Japanese).

[12] A. Hanada, K. Minomo, A. Nakamura, Y. Nishida, Y. Amano, K. Kobayashi, E. Nakasu, K. Watanabe, and K. Enami, "Development of MPEG-2 Bitstream Processor for Digital Terrestrial Services, " ITE Annual Convention, 8–2, 2002 (in Japanese).

[13] Y. Honma, E. Yasuda, and S. Miyazawa, "Development of High-Compression HDTV Encoder for Digital Terrestrial Broadcasting," Broadcasting Technologies, No. 7, pp. 119–124, 2003 (in Japanese).

[14] K. Nakamura, T. Yoshitome, and Y. Yashima, "Super High Resolution Video CODEC System with Multiple MPEG-2 HDTV CODEC LSIs, ISCAS2004," Vol. III, pp. 261–264, and pp. 793–796, 2004.

[15] H. Miyahara, M. Hidaka, M. Chiku, M. Nanbu, F. Nidaira, and M. Aso, "Development of High Definition Camcorder for Consumer," ITE Annual Convention, 9–2, 2003 (in Japanese).

[16] M. Inamori, H. Iwasaki, T. Onishi, M. Ikeda, J. Naganuma, and Y. Yashima, "New Set-top Box for Interactive Visual Communication using MPEG-2 Full-duplex CODEC LSI," ICCE2005, pp. 335–336, 2005.

[17] "Successful development of a H.264 real-time CODEC LSI for the contribution of broadcasting use," NTT News Release, April 6, 2007. http://www.ntt.co.jp/news/news07e/0704/070406a.html

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