Historical Overview of Semiconductor Device Reliability for Telecommunication Networks—

Field Data, Prediction Model of Device Failure Rate, and Wear-out Failure Analyses at NTT

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Abstract

The 1960s brought about the advent of the intense development of semiconductor devices for industrial and commercial applications. Since then, NTT has taken the initiative in introducing semiconductor devices into telecommunication networks to realize highly reliable and miniaturized equipment with high performance.

This article reviews the failure physics approach we have been using to develop highly reliable semiconductor devices. It also summarizes our findings regarding device failures in field use and discusses a failure rate prediction model based on the findings.

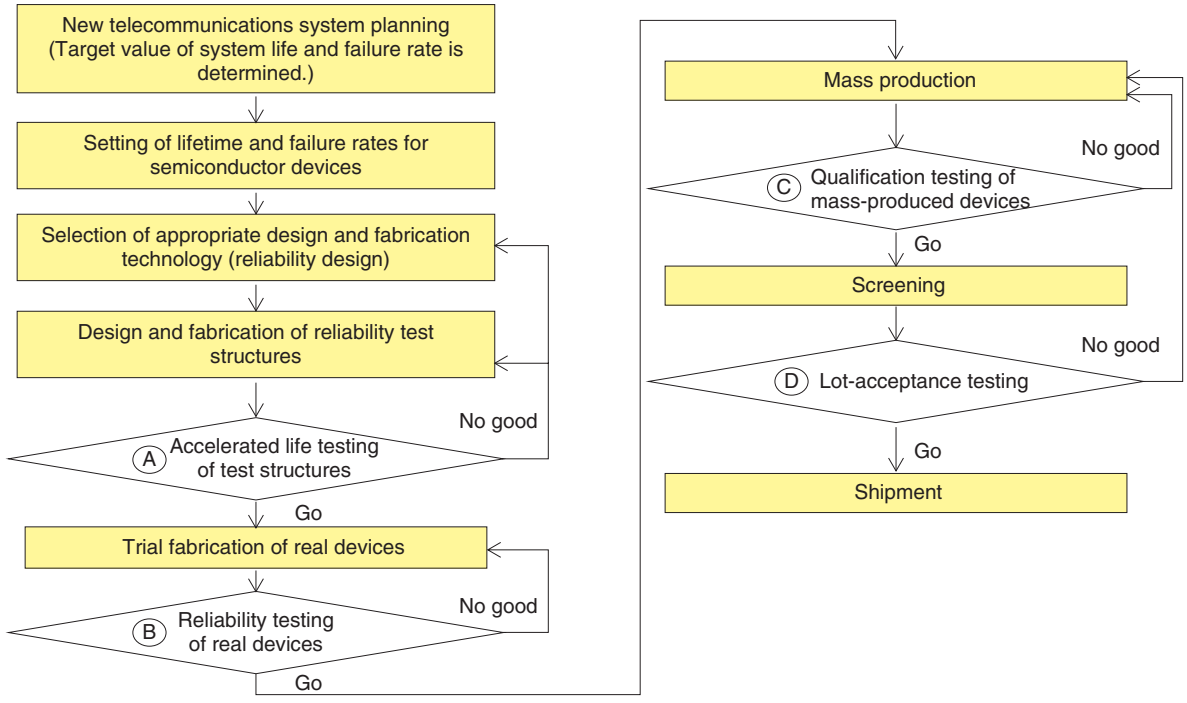
1. Introduction

From the 1960s to the 1980s, NTT's use of semiconductor devices was the primary factor in the successful development of highly reliable and miniaturized high-performance telecommunications equipment. In the 1960s, the semiconductor industry was in its infancy. Therefore, it was not really known how reliable semiconductor devices would be, and experience in using them in telecommunications equipment was lacking. At that time, NTT was the first company in the world to introduce transistors into telecommunications equipment [1]–[7].

In the early 1960s, NTT introduced a failure physics approach (also known as *the physics of failure*), described in the next section, in order to develop highly reliable semiconductor devices for telecommunications equipment. The target values for device reliability required in network system design were a lifetime longer than 25 years and a failure rate lower than 0.2–150 FIT (failure in time, which is defined as the number of failures per billion device hours (10^{-9}/h)), depending on the type of device (from diodes to LSIs (large-scale integrated circuits)) and the kind of equipment [4]. For semiconductor devices that had been developed at that time, accelerated life tests (longer than 10,000 hours) and long-term operation tests at room temperature using a large number of devices were conducted to confirm that those targets had been achieved. In addition, field failure tests were carried out with actual working equipment to confirm the high reliability of semiconductor devices and of passive and mechanical components as well.

On the basis of the results of those field failure tests, we developed a failure rate prediction model for electronic components including semiconductor devices to use in the reliability design of the next stage of our telecommunications equipment [8], [9]. The objectives of this failure rate prediction model were the same as those of the well-known MIL-HDBK-217 (Military Handbook) model for reliability prediction of electronic equipment [10], and the procedures were similar.

The development of reliability assurance standards



Criteria for each testing point:

A	B	C	D
- Failure mode extraction using test structures - Whether the estimated failure rate is lower than the target value or not	- Whether degradation modes are a matter or not - Whether lifetime and failure rate of wear-out failures are lower than the target values or not	- Whether lifetime and failure rate are lower than the target values for mass-produced devices or not	- Whether the produced lot is normal or not

Fig. 1. Procedure for developing highly reliable semiconductor devices for telecommunications equipment.

such as MIL-STD (Military Standard) -19500 [11] and MIL-STD-38510 [12] started in the late 1950s, and NTT applied them to semiconductor devices installed in NTT equipment to ensure their high reliability [8]. Over the years, NTT also developed and periodically revised its own assurance standards to reflect advances in device technology. These standards were finally withdrawn in 1987 because the reliability of semiconductor devices had been improved to the level where such standards were no longer necessary.

2. Development of highly reliable devices based on the failure physics approach

The failure physics approach for developing highly reliable devices is as follows; first, various failure modes are investigated in accelerated life tests. Next, associated failure mechanisms are clarified, and device reliability is improved by optimizing device structures and fabrication processes. Finally, a reliability assurance procedure is carried out; this procedure includes conducting wafer acceptance tests, screening tests of encapsulated devices for eliminating early failures, and lot-acceptance tests.

The procedure we followed for developing highly reliable semiconductor devices is shown in **Fig. 1**, and examples of devices used in NTT equipment are summarized in **Table 1** [13], [14]. The relationship between failure rate and working time is known as the bathtub curve, which depicts the early failure period, random failure period, and wear-out failure period. Early failures are caused by latent defects induced during fabrication, and the failure rate decreases with time ($\beta < 1$, where β is the shape parameter in a Weibull distribution). Random failures are caused by

Table 1. Main devices used in various telecommunication systems, failure modes, and countermeasures for higher reliability.

System (System name/ year installed)	Main devices (type or process used)	Main failure modes	Countermeasures for higher reliability
Coaxial cable transmission system (CP-12MTr/1967)	Bipolar transistors (direct wire bonding on metallization of E-B junction)	- Wire bond breakage due to Au-Al compound formation between Au wire and Al metallization pad on junction - E-B junction short due to Au penetration of Au wire into junction	- Control thermal process during wire bonding and control bond strength - Change Au wire to Al wire
Electronic exchange system (D10/1972)	Logic ICs (bipolar CSL type)	- Open failure of Al metallization due to corrosion	- Improve passivation film
Electronic exchange system (D10-HCP/1977)	4K DRAM (n-channel MOS process)	- Increase in leakage current - Decrease in holding time	- Control contamination - Optimize screening conditions
Submarine coaxial cable system (CS-36M/1977)	Bipolar transistors (Au/Pt/Ti electrode, BeO substrate for high thermal conductivity)	- Metal penetration into junction - h_{FE} degradation	- Improve electrode metal structure from Al to Ti/Pt/Au electrode - Improve passivation film from single layer of SiO_2 to SiO_2/SiN - Use individual device assurance method
Digital electronic exchange system (D70/1982)	High-voltage bipolar LSIs (dielectric isolation, pn junction isolation, plastic encapsulation)	- Open failure of Al metallization due to corrosion - Degradation of breakdown voltage for isolation	- Adopt SiN passivation film - Adopt EPIC dielectric isolation structure combined with field plate
	64K DRAM	- Soft error	- Use chip coating with resin - Adopt ECC technique
Optical fiber transmission system (F-400M/1983)	InGaAsP/InP BH-LDs (Fabry-Perot type, buried-heterostructure)	- Increase in thermal resistance in die bonding to substrate - Short failure due to Sn whisker growth around die bonding - Degradation of optical power output	- Improve metallized layer and adopt silicon heat sink - Use Au-rich AuSn die bonding - Use individual device assurance method
ISDN network (ISDN/1988)	Submicrometer custom LSIs (CMOS, BiCMOS)	- Open failure due to electromigration and stress migration of Al metallization - Vth degradation due to hot-carrier effect - TDDB of gate oxide	- Use multilayer metallization structure (Al-Si-Cu/Ti/TiN/Ti, etc.) - Control process of H_2O content in interlayer dielectric film - Use high-voltage and low-temperature screening

BeO: beryllium oxide
BH: buried heterostructure
CSL: controlled saturation logic
Cu: copper
E-B: emitter-base
ECC: error-correcting code
EPIC: epitaxial passivated integrated circuit
H_2O: hydrogen dioxide (water)
InGaAsP: indium gallium arsenide phosphide
ISDN: integrated services digital network
Pt: platinum
$Si0_2$: silicon dioxide
SiN: silicon nitride
Sn: tin
TDDB: time-dependent dielectric breakdown (gate oxide breakdown)

small latent defects that occur after relatively long-term operation at a constant failure rate ($\beta = 1$). Wear-out failures occur after long-term operation due to wear-out and fatigue, and the failure rate tends to

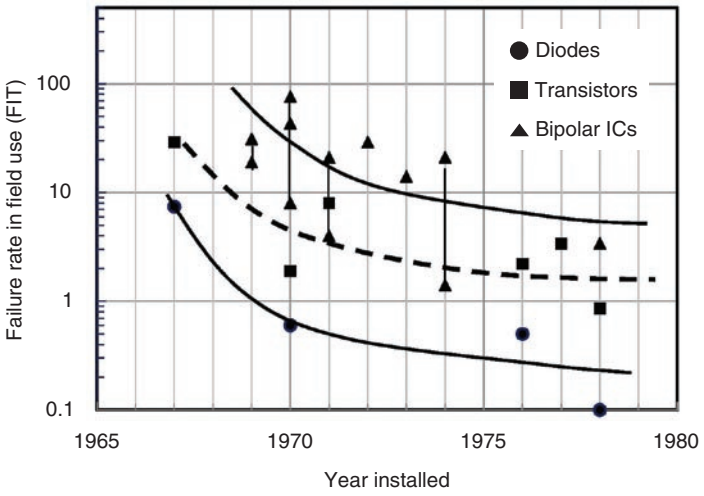


Fig. 2. Failure rate in field use vs. year installed in NTT equipment for semiconductor devices.

increase rapidly during this period ($\beta > 1$).

Countermeasures consisting of fabrication process control and proper screening were effective in reducing the failure rate of early failures. For random failures, long-term tests conducted under actual working conditions confirmed that failure rates were lower than the target value. Wear-out failures, which should never occur during the guaranteed lifetime of a device, were prominent for miniaturized LSIs and optical devices. These failures are classified into degradation-related failures and catastrophic ones. Examples of degradation failures are a decrease in the optical output power of laser diodes (LDs) or changes in the current gain (h_{FE}) of bipolar transistors during operation. In a circuit affected by such degradation, the extent of the degradation has to be accurately estimated in order to analyze its effect on circuit operation in the intended working conditions. Examples of catastrophic failures are the lifting of Au (gold) wire bonding and stressmigration in Al (aluminium) interconnections in plastic-encapsulated LSIs. Wear-out failure analyses that we performed for plastic encapsulated LSIs and LDs are described in more detail in section 4.

3. Failure rate in field use and reliability prediction model

3.1 Failure rate data in field use

From the 1960s to the 1980s, NTT collected a large amount of data on field failures of devices in NTT telecommunications equipment. The devices were typically operated in an air-conditioned room with a maximum junction temperature of 55ºC (ambient temperature 40ºC) and relative humidity of 20–70% [5], [15]–[25].

The relationships between the failure rate of devices (in failures/10^9 hours = FIT) in field use and the installation year for diodes, bipolar transistors, and bipolar integrated circuits (ICs) are shown in **Fig. 2**. These values were selected from field data of more than 1×10^{10} device·hours for diodes, 4×10^9 device·hours for bipolar transistors, and 5×10^8 device·hours for bipolar ICs, which corresponded to one to three years of operation. The lower limits of the failure rate estimation are 0.01 FIT for diodes, 0.25 FIT for transistors, and 2 FIT for bipolar ICs. These lower limits are one order lower than the observed failure rate as described below.

As shown in Fig. 2, the failure rate decreased with time and approached a certain constant value depending on the device group. These curves are similar to the so-called learning curve, and the constant value corresponds to the failure rate in the random failure period for mature devices. The failure rate seemed to become higher as the process complexity increased. The failure rate in the random failure period was estimated to be about 0.2 FIT for diodes, about 2 FIT for transistors, and about 5 FIT for bipolar ICs. The failure rate observed in field use from the 1960s to the 1980s for more precisely divided device groups in the random failure period is plotted in **Fig. 3**. The figure shows that somewhat high failure rates were observed for metal-oxide semiconductor (MOS) ICs, which

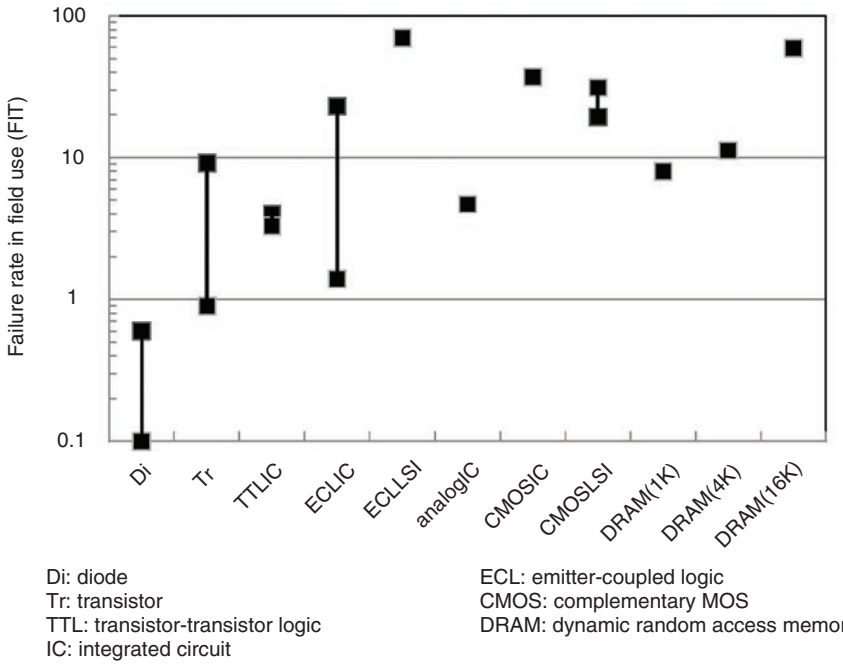


Fig. 3. Failure rate in field use in random failure period for various semiconductor devices.

had just been developed and had not yet matured in those days, though the failure rates were less than 100 FIT. We also examined the failure rate for LSIs developed in the 1990s by conducting accelerated life tests with a large number of LSIs for about 3000 hours. We found that the failure rates of memory LSIs such as 64-K–1-M DRAM (dynamic random access memory) were below 100 FIT, and those of CMOS (complementary MOS) logic LSIs (about 150-K gates) fabricated with 0.25–0.5 μm technology were below 200 FIT. The failure rates of these LSIs were expected to decrease in the accelerated life tests and approach a constant value below 100 FIT if the tests were continued beyond 3000 hours, because no failures were observed within the first 3000 hours.

3.2 Failure rate prediction models

3.2.1 NTT model

A failure rate prediction model was developed on the basis of the collected field data and used in the next stage of equipment design [8], [9], [26], [27]. The NTT failure rate prediction model (called the NTT model hereafter) was sought to determine the constant failure rates in the random failure period and was similar to the well-known MIL-HDBK-217 model. It was established for semiconductor devices and passive and mechanical components used for NTT equipment. The failure rate of ICs is expressed as

$$\lambda = \lambda_b \cdot \pi_Q \cdot (\pi_E + \pi_T \cdot \pi_V), \quad (1)$$

where λ is the predicted failure rate, λ_b is the basic failure rate (FIT), π_Q is the quality factor, π_E is the environmental factor, π_T is the temperature factor, and π_V is the power supply voltage factor.

The basic failure rate λ_b was defined for each device type, integration level, and technology. For example, the λ_b of bipolar digital logic ICs and MOS DRAM is listed in **Table 2**.

Quality factor π_Q was given a value from 1 to 4, depending on the quality grade defined by NTT; it was 1 for highly reliable ICs (namely, quality-controlled devices used in NTT equipment). Environmental factor π_E was given a value from 0.3 to 1.8, depending on the operating environment such as an air-conditioned room, vehicle, or mobile telephone; it was 0.3 for an air-conditioned room. Power supply voltage factor π_V was expressed as $\pi_V = 0.35 \times \exp(0.21V_{DD})$ for CMOS ICs and 1 for other devices.

Temperature factor π_T is given as

$$\pi_T = \exp\left(\frac{0.3}{k}\left(\frac{1}{339} - \frac{1}{273+T_j}\right)\right) + \exp\left(\frac{0.7}{k}\left(\frac{1}{356} - \frac{1}{273+T_j}\right)\right), \quad (2)$$

Table 2. Example of basic failure rate of ICs.

Category	λ_b (FIT)					
Bipolar digital logic ICs	5.0	for	Q ≦ 100	$0.50Q^{0.50}$	for	Q ≧ 100
MOS DRAM	$3.81B^{0.25}$	for	B ≦ 16 K	$0.337B^{0.50}$	for	B ≧ 16 K

Q: number of active transistors
B: bits; K = 1024

where k is Boltzmann's constant and T_j is junction temperature at the operating condition. This formula was derived by considering the contribution to the failure of two activation energies (Ea) of 0.3 and 0.7 eV. Here, various failure mechanisms showed different activation energies, and the major failure mechanisms for MOS ICs were gate oxide breakdown (TDDB) with Ea=0.3 eV and electromigration or stressmigration of metallization with Ea=0.7 eV. Activation energies for these major failure mechanisms were therefore introduced to define the temperature factor in the NTT model.

Unlike the MIL-HDBK-217 model, the NTT model considered the effect of packaging only for hermetic or non-hermetic (plastic-encapsulated) sealing and did not take the effect of package type or size into account.

3.2.2 Comparison of NTT model with other failure rate prediction models

The final revised version of the NTT model was completed in 1981 and published in 1982 [8]. In those days, comparable prediction models for electronic components were MIL-HDBK-217 (version C (1979) and version D (1982)), and Bellcore TR-332 [28]. Later, other failure rate prediction models were developed such as PRISM [29] and IEC/TR (International Electrotechnical Commission/Technical Report) 62380 [30]. These models consider not only individual components but also the total system operation, and they differ from device-oriented models such as the NTT model and MIL-HDBK-217. Quantitative comparisons of the predicted trend of failure rates among these various models were needed but had not been carried out [31], [32]. We therefore performed comparisons between six device-oriented models of the NTT model (1981), three versions of the MIL-HDBK-217 model (C(1979), E(1986), F(1991)), and two versions of the Bellcore model (TR-332 issue (1997), SR-332 issue 2 (2006)). (Note that TR-332 was changed to SR-332 in 2001.) Operating conditions were assumed to be T_j = 55ºC (ambient temperature of 40ºC) and an air-conditioned room, which corresponded to "Ground, Benign" in MIL and also to the NTT electronic switching system environment. The quality grade was selected as the highest reliable level at NTT, i.e., $\pi_Q = 1$, which was equivalent to MIL-class B. The power supply voltage factor was a standard voltage, and $\pi_V = 1$. Under these conditions, comparisons of failure rate were performed for NMOS (n-channel MOS) DRAM and bipolar digital logic ICs as a function of the scale of integration. The results are shown in **Figs. 4** and **5**.

For DRAM, the failure rate prediction curve obtained with the NTT model lies between MIL-HDBK-217 C(1979) and 217 E(1986), and the relationship between failure rate and DRAM size seems to shift in parallel with subsequent versions, i.e., the year of publication. For digital logic ICs, the prediction curves tend to converge at around 200 FIT with increases in the number of gates, regardless of the model. The features of the relationship between failure rate and scale for DRAM are somewhat different from those for bipolar logic ICs. This difference can be explained as follows; the process technology for DRAM had been revised with the very large scale production more quickly than it had for bipolar logic ICs. Consequently, the yield and reliability were improved more quickly compared with bipolar digital ICs. The trend in the predicted results indicated that the failure rate of LSIs would converge to a constant value regardless of the scale of integration, and that value was estimated to be 100–200 FIT even for the maximum scale of integration for a given year. On the whole, the relationship between failure rate and scale of integration can be assumed to shift in parallel with the fabrication year due to advances in technology. Although these prediction models involving the NTT model are old, they can still be used as references for predicting failure rates of recently developed devices.

4. Examples of analyses for wear-out failure modes

Wear-out failure is divided into catastrophic failure

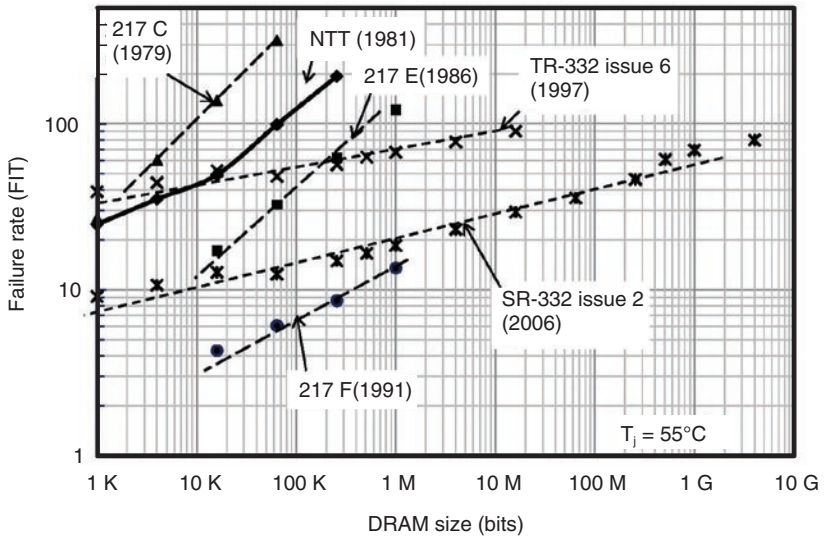


Fig. 4. Predicted failure rate vs. size of DRAM for various failure rate prediction models.

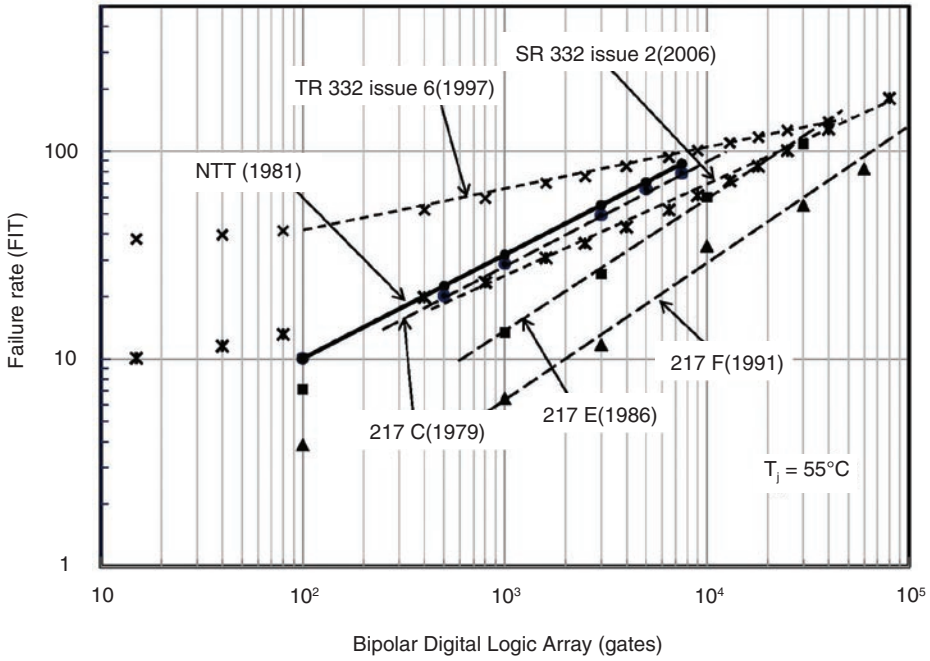


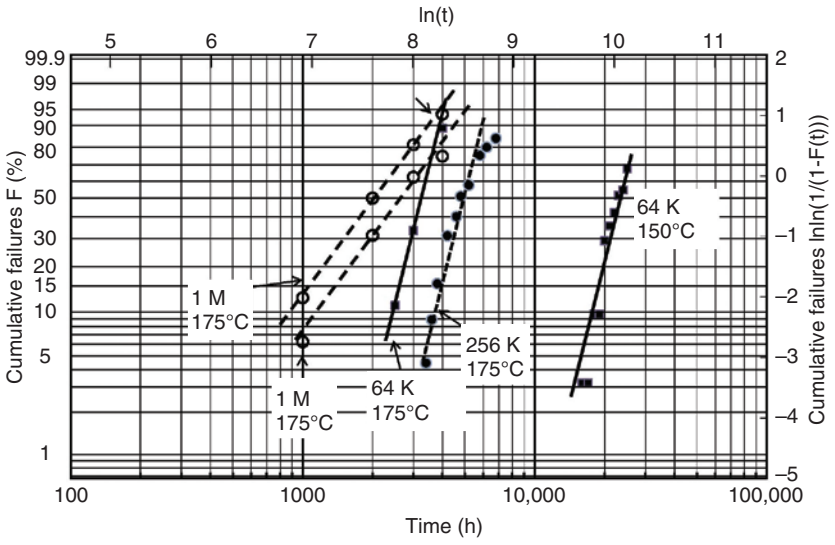
Fig. 5. Predicted failure rate vs. number of gates in bipolar logic IC gate arrays for various models.

and degradation failure modes, as mentioned previously. The time to reach wear-out failures has tended to decrease with the rapid progress in the miniaturization of device dimensions used in LSIs since the latter half of the 1980s. Reliability analyses of plastic-encapsulated LSIs and LDs are described below as respective examples of catastrophic and degradation failures.

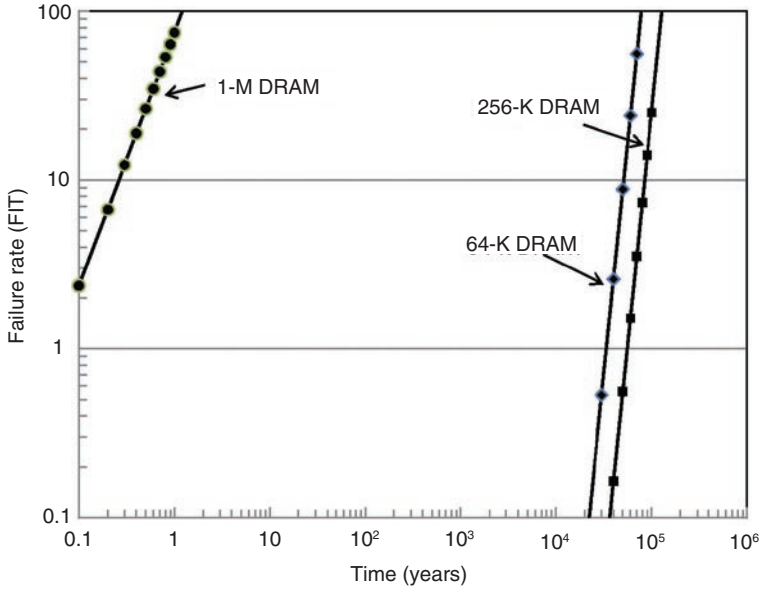
4.1 Reliability analysis for catastrophic failures

A reliability analysis was carried out for plastic-encapsulated MOS DRAMs, in which typical failure

modes were open failures caused by the lifting of Au wire-bonds and stressmigration of Al(Si) metallization [13]. Weibull plots of failures observed in high-temperature operating tests for 64-K, 256-K, and 1-M DRAMs are shown in **Fig. 6**. Failure analyses clarified that the failures involved the lifting of Au wire-bonds for the 64-K and 256-K DRAM and stressmigration of Al(Si) metallization for the 1-M DRAM. Au wire-bond failures were induced by thermal expansion mismatch among the molding compounds (10–20 ppm/ºC), Au wire (14 ppm/ºC), and Si (3 ppm/ºC), and also by decreases in the thermal expansion coefficient of molding compounds during high-temperature aging. Stressmigration failure was



(a) Weibull failure distribution



(b) Failure rate vs. time in use

Fig. 6. (a) Failures observed for plastic encapsulated DRAM in high-temperature operation tests and (b) estimated failure rate vs. time under normal operating temperature (T_j = 55ºC).

Table 3. Weibull parameters determined from high-temperature operation tests for NMOS DRAM.

Device	η (scale parameter) at 175°C (h)	β (shape parameter)	Activation energy (eV)	Failure mode (open failure)
64-K DRAM	3400	6.5	1.25	Lifting of Au wire-bonds
256-K DRAM	5200	6.5	1.25	Lifting of Au wire-bonds
1-M DRAM	2300	2.5	0.55	Stressmigration of Al(Si) interconnection

caused by tensile stress due to the thermal expansion difference between the Al interconnection and the intermediate layer.

Weibull parameters determined from the results of the accelerated life tests shown in Fig. 6(a) are listed in **Table 3**. The values of the shape parameter β were 6.5 for 64-K and 256-K DRAM and 2.5 for 1-M DRAM, which indicates the wear-out failures. The activation energy of the Au wire-bond open failure was estimated to be 1.25 eV for 64-K DRAM, and was assumed to be the same for the 256-K DRAM. The activation energy of the Al(Si) stressmigration failure observed in the 1-M DRAM in the 150ºC and 175ºC tests was estimated to be 0.15 eV. However, the failure rate for stressmigration was known to have a plateau around 180ºC and to show complicated temperature dependence [33]. Therefore, 0.55 eV was adopted as the activation energy for failure rate estimation, in which the energy was derived from testing below 150ºC using other test structures [34].

The relationship between estimated failure rate and operating time at the operating temperature of 55ºC derived from the above parameters is shown in Fig. 6(b) in a Weibull distribution. Here, the failure rate in the Weibull distribution was obtained by

$$\lambda(t) = \left(\frac{\beta}{\eta}\right)\left(\frac{t}{\eta}\right)^{\beta-1} \quad (3)$$

The target value of the failure rate for catastrophic wear-out failures was set at 10 FIT after 25 years. The failure rates of 64-K and 256-K DRAM were far below the target value, while that of the 1-M DRAM reached the target value after only one year, as shown in Fig. 6(b), which indicates an obvious need for improvement. The1-M DRAM was subsequently improved by using Al(Si, Cu) interconnections instead of Al(Si) interconnections, and the lifetime of the improved 1-M DRAM was confirmed to be 100 times longer than the former one.

Further, room-temperature operating tests were carried out over 17,400 hours with 320 samples, and the results confirmed that the rates of random failures of 64-K DRAM were below 165 FIT. For the 1-M DRAM, 150ºC operating tests using 110 samples for a duration of 10,000 hours confirmed that the rates of random failures were below 62 FIT. The analyses of wear-out failures and random failures confirmed that the total failure rates satisfied the target values.

4.2 Reliability analysis for degradation failures

Degradation of electrical characteristics is a major concern for semiconductor devices such as LDs, whose optical output power degrades with time. Degradation analyses, therefore, are needed in addition to random failure examination and are typically obtained by conducting accelerated life tests. It is imperative to confirm that the amount of degradation during the guaranteed duration of use is within the designated value by analyzing the degradation characteristics. A reliability analysis was done to determine the characteristic degradation of LDs used in the FS-400M submarine optical telecommunications system.

Samples were Fabry-Perot buried type InGaAsP-LDs with a 1.3 μm wavelength. In actual applications, an automatic power control (APC) circuit was used to maintain a constant optical output power; i.e., degradation of the constant output power of LDs was maintained by the increase in driving current in the APC circuit. The failure criterion of the LD degradation was normally defined by a 50% increase in driving current. The accelerated life tests were conducted in conditions of 50ºC and 70ºC temperatures with an output power of 5 mW, and also at 10ºC and 5 mW, which was the actual operating condition. In total, 1000 samples were tested, with 100 samples used for the 10ºC test, 800 samples for the 50ºC test, and 100 samples for the 70ºC test. The rate of random failures was also estimated by testing the same 1000 samples [35].

4.2.1 Degradation mode of electrical characteristics

The degradation mode was a decrease in optical output power, and the degradation corresponded to an increase in the driving current in the APC circuit, which could be easily monitored. The typical

degradation characteristics in the 70ºC test are shown in **Fig. 7**. The driving current increased with time as $\Delta I_d/I_o\,(t) \propto t^n$, where ΔI_d is the increase in driving current, I_o is the initial driving current, t is the test time, and n is a constant. The value of n varied with the samples in the range of 0.4–1.0. The lifetime, which is defined as the time to reach a 50% increase in driving current, was estimated by extrapolating the relation shown in Fig. 7 for each sample. A log-normal plot of cumulative failures versus lifetime for the 70ºC operating test is shown in **Fig. 8(a)**. This log-normal distribution was approximated by the median life of $\mu = 1.4 \times 10^5$ hours and the standard deviation of $\sigma = 0.99$, except for the long lifetime portion. Although the activation energy was estimated to be about 0.8 eV from the data at 50ºC and 70ºC, the lowest activation energy of 0.35 eV used in semiconductor devices was applied in order to obtain a more severe prediction in the actual lifetime estimation. The failure rate is given by the following equation for the log-normal distribution [36]:

$$\lambda(t) = \frac{\sqrt{2}\cdot\exp\left\{-\frac{1}{2\sigma^2}\cdot\left(1n\left(\frac{t}{\mu}\right)^2\right)\right\}}{\sqrt{\pi}\cdot t\cdot\sigma\cdot\mathrm{erfc}\left(\frac{1}{\sqrt{2}\sigma}\cdot 1n\left(\frac{t}{\mu}\right)\right)}. \quad (4)$$

The estimation of failure rate versus time (years) at 10ºC in the actual undersea environment is shown in **Fig. 8(b)**. From this plot, a failure rate of 220 FIT after 25 years was estimated, while 0.001 FIT after 25 years was estimated when 0.8-eV activation energy was applied.

4.2.2 Random failure mode

Long-term reliability testing for 19,000 hours at maximum was carried out for 1000 samples as described above. Except for optical output degradation, no catastrophic failures were observed in these tests. A failure rate lower than 13 FIT (CL=60%) was estimated from these tests of 7.3×10^7 device·hours at 10ºC, where 0.35-eV activation energy was used. Thus, the total rate of wear-out failure and random failure was estimated to be below 233 FIT, which was below the target value of 300 FIT at 10ºC operation and 25 years duration.

4.2.3 Screening

The operating test results showed a relatively good correlation between the increase in driving current at 1000 hours and the lifetime estimated using the procedure described above with a correlation coefficient of -0.62. This indicates that a failure rate one order of

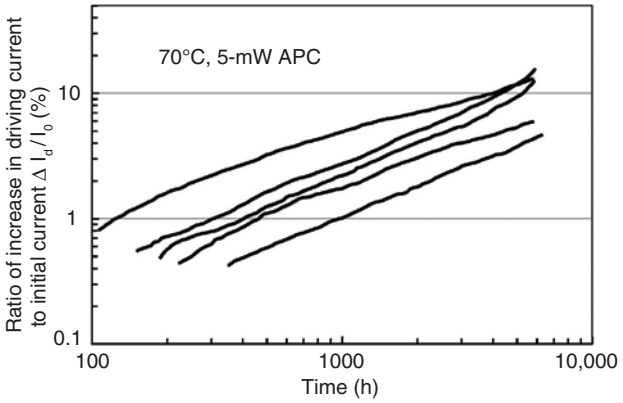
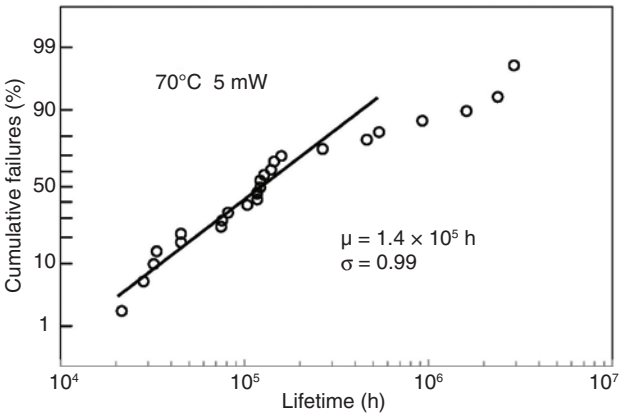
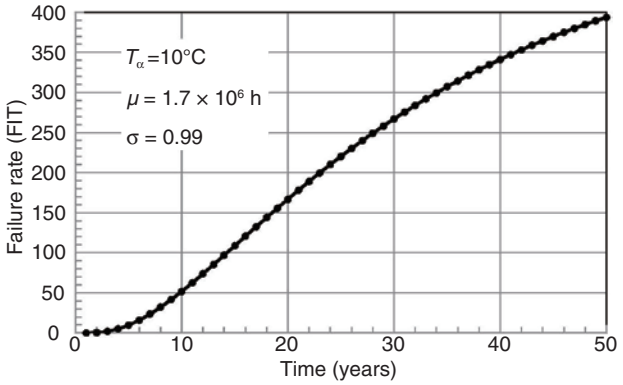


Fig. 7. Driving current degradation of LDs used in FS-400M system during high-temperature operating test.



(a) Log-normal failure distribution



(b) Failure rate vs. time (years)

Fig. 8. (a) Lifetime distribution of LDs derived from Fig. 7 and (b) failure rate prediction at 10°C (failure criterion is 50% increase in driving current).

magnitude lower than 300 FIT could be obtained by selecting LDs with a smaller increase in driving current after 1000 hours of aging. This procedure was implemented as the third step of screening, where the total screening consisted of three steps: 70ºC/150 mA for 100 h, 70ºC/8 mW with APC for 100 h, and 70ºC/5 mW with APC for 1000 h [35]. The first and second steps were used to avoid early failures and stabilize the electrical characteristics, and the third step was done to select a long-lifetime device. This screening method was called the *individual device assurance method* because the electrical characteristics of each LD at all stages of production and screening were acquired individually, and because it was expected that this method would make it possible to select LDs with better stability and longer lifetime. This individual device assurance method was also applied for the selection of bipolar transistors used in the submarine coaxial transmission system (CS-36M), in which transistors with high stability, i.e., degradation of h_{FE} of less than 3%, were required during the intended duration of service [37].

4.3 Future challenges

Recently, wear-out failure has become the most significant issue in the reliability of advanced LSIs because the process dimensions have been miniaturized to a size of about several tens of nanometers, and thin plastic encapsulation of high pin counts has been applied, which results in shorter lifetimes. For optical semiconductor devices, the time to a wear-out failure such as the degradation of optical output power has been the most important issue ever since the introduction of optical devices. For such devices, there is a need for more precise reliability analyses and accurate failure rate estimation for both catastrophic failure and degradation modes.

In line with the recent ITRS (International Technology Roadmap for Semiconductors) [38], it has been proposed that the failure rate for long-term reliability should be determined according to system scale. For example, 1000 FIT/chip is required for one chip/system, while 1 FIT/chip is needed for 1000 chips/system. However, 1 FIT/chip is not reasonable because it is very difficult or even impossible to ensure by reliability testing when considering the device·hours and testing cost. The future challenge in ensuring high reliability of advanced devices is to provide the most accurate reliability information based on the advanced failure physics approach to system designers, who will then be able to design reliable systems by introducing a redundant unit such as multiple devices used in parallel.

5. Summary

This article presented a review of the development of highly reliable semiconductor devices used in NTT telecommunications equipment over a period of several decades. The findings obtained and the future challenges are summarized as follows:

(1) Highly reliable semiconductor devices were developed through the failure physics approach and were assured through accelerated life testing and field failure examination to have a lifetime longer than 25 years and failure rates from 0.1 to150 FIT (depending on device type), which were adequate for application to NTT telecommunications equipment.

(2) Field failure data for semiconductor devices were collected for various types of operating equipment from the 1960s to 1980s. The data revealed that the failure rate decreased with time and tended to approach a constant value of less than about 100 FIT regardless of the device type or scale of integration.

(3) The failure rate prediction model, called the NTT model, was developed based on field failure data collected and used in equipment reliability design. Comparisons between the NTT model and other models used in those days, e.g., MIL-HDBK-217 and Bellcore TR-332, showed almost the same prediction results.

(4) Since wear-out failure modes vary with device type or technology, it is necessary to clarify failure modes and failure mechanisms for relevant devices by conducting accelerated life tests and failure analyses, and to predict accurate failure rates in actual-use conditions. The use of such accurate failure rate data will lead to the design of reliable equipment.

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