Regular Articles

High-sensitivity Avalanche Photodiode and Receiver Optical Subassembly Technology for 100-Gbit/s Ethernet

Fumito Nakajima, Masahiro Nada, and Toshihide Yoshimatsu

Abstract

We have developed a 25-Gbit/s avalanche photodiode (APD) with an inverted p-down, triple mesa structure and a 100-Gbit/s (4 × 25-Gbit/s) APD receiver optical subassembly (APD-ROSA). The APD-ROSA includes a monolithic four-channel APD array and an ultrasmall planar-lightwave-circuit demultiplexer. In a performance evaluation, the APD achieved a record minimum receiver sensitivity of –20 dBm and 50-km error-free transmission without an optical amplifier.

Keywords: avalanche photodiode (APD), 100-Gbit/s Ethernet, receiver optical subassembly (ROSA)

1. Introduction

The rapid increase in the capacity of communication networks has led to many new services. To handle the growing amount of transmitted data, the Ethernet standard has been repeatedly extended [1], and faster and faster interface speeds are necessary in order to cope with this trend. In particular, datacenters will need to deal with ever-increasing amounts of data in limited areas, and at the same time, the capacity of optical components and reductions in their size and power consumption will be urgently required. In addition, the transmission distance of 100-Gbit/s Ethernet systems will also need to be extended in order to meet the requirements for future application areas. Extending the reach beyond 10 km is very important for telecom carriers because it will enable most inter-building networks to be covered.

The key to extending the distance is the optical receiver because the launch power of the laser diode in the transmitter is limited. A schematic image of a 100-Gbit/s Ethernet 10-km transmission system (100GBASE-LR4) that uses a transmission optical subassembly (TOSA) and receiver optical subassembly (ROSA) is shown in **Fig. 1(a)**. A typical ROSA includes a PIN photodiode to convert optical signals to electrical signals. The receiver sensitivity of a ROSA is limited in the system, and therefore, to extend the transmission distance, it is necessary to use an optical amplifier such as a semiconductor optical amplifier (SOA) in front of the ROSA, as shown in **Fig. 1(b)**. However, in this configuration, the receiver module size cannot be reduced enough to keep up with the expected size of packages such as that of a CFP4 transceiver. In addition, an SOA consumes as much as several watts of power and enlarges the footprint.

Thus, to provide a means of improving the sensitivity without increasing the package size, we proposed a novel high-speed avalanche photodiode (APD) [2], as shown in **Fig. 1(c)**. An APD has an internal gain that improves the sensitivity by several decibels compared to that of a PIN photodiode. Our APD, called an inverted p-down APD, has achieved a high multiplied
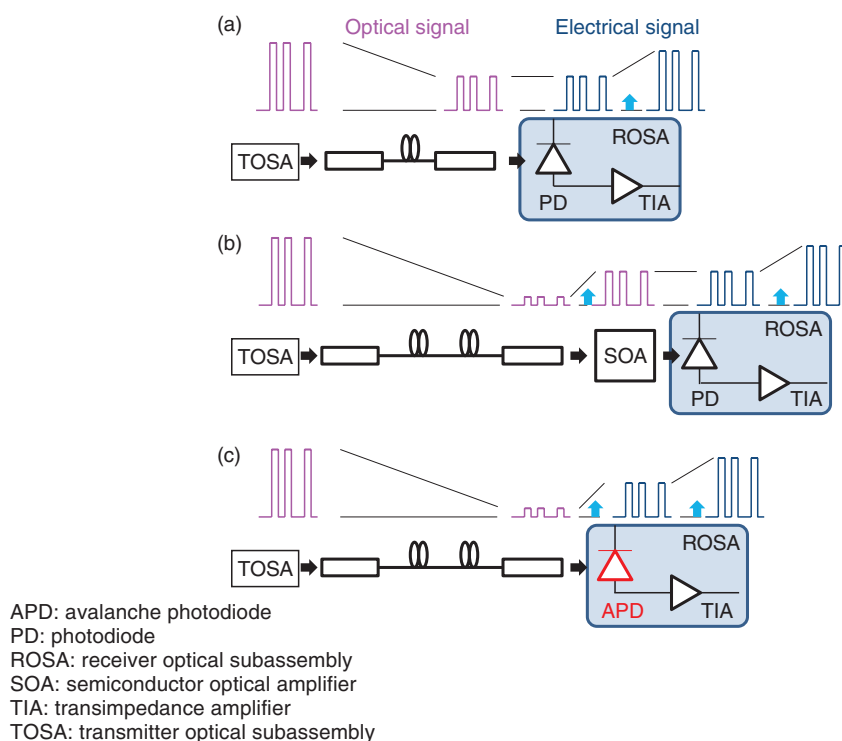
Fig. 1.   100-Gbit/s Ethernet transmission systems using TOSA and ROSA.

responsivity-bandwidth product of 18.5 × 9.1 = 168 A/W·GHz [3] and can operate with a bandwidth large enough for receiving 25-Gbit/s data. In this article, we describe the design and fabrication of the high-speed, stable APD and the results of applying it to a 100-Gbit/s four-channel APD-ROSA.

2.   Inverted p-down APD

In addition to large bandwidth and high responsivity, the reliability and stability of an APD are the most important factors for its practical application, since a high applied voltage is necessary to obtain sufficient internal gain. We have devised a simple new APD structure, the inverted p-down APD, that is suitable for even higher speeds by scaling the structure down. The simple structure confines the electric field, which makes it possible to obtain good stability.

A schematic cross section of our APD is shown in **Fig. 2(a)**. The epitaxial layers were grown on a semi-insulating InP substrate by using MOCVD (metal organic chemical vapor deposition). The APD structure consists of a p-doped contact layer, p-doped and undoped InGaAs absorption layers, an InAlAs avalanche layer sandwiched between p- and n-doped

field control layers, and an n-doped contact layer.

Although there is a trade-off between bandwidth and responsivity in an APD, we optimize the thickness relationship between the p-doped and undoped absorption layers to relax the trade-off, in accordance with the concept of MIC (maximized induced current) design [4]. This is necessary because the two types of photo-excited carriers, namely holes and electrons, are transported through the p-doped and undoped layers by different mechanisms. We show how the calculated responsivity and the calculated intrinsic 3-dB-down bandwidth for a multiplication factor (M) of 1 varies with the total thickness of the absorption layer in **Figs. 2(b)** and **2(c)**. The optimum intrinsic 3-dB-down bandwidth was achieved by tuning the proportion of the total absorption layer occupied by p-doped absorption. For a speed of 25 Gbit/s, a total thickness of 1.0 μm provides a sufficiently large bandwidth and a high responsivity of 0.9 A/W.

Furthermore, the gain-bandwidth product (GBP) is one of the most important factors to define the APD receiver sensitivity. Making the InAlAs avalanche layer thinner increases the GBP; however, it also increases the tunneling current density. Because a larger tunneling current degrades the optical receiver
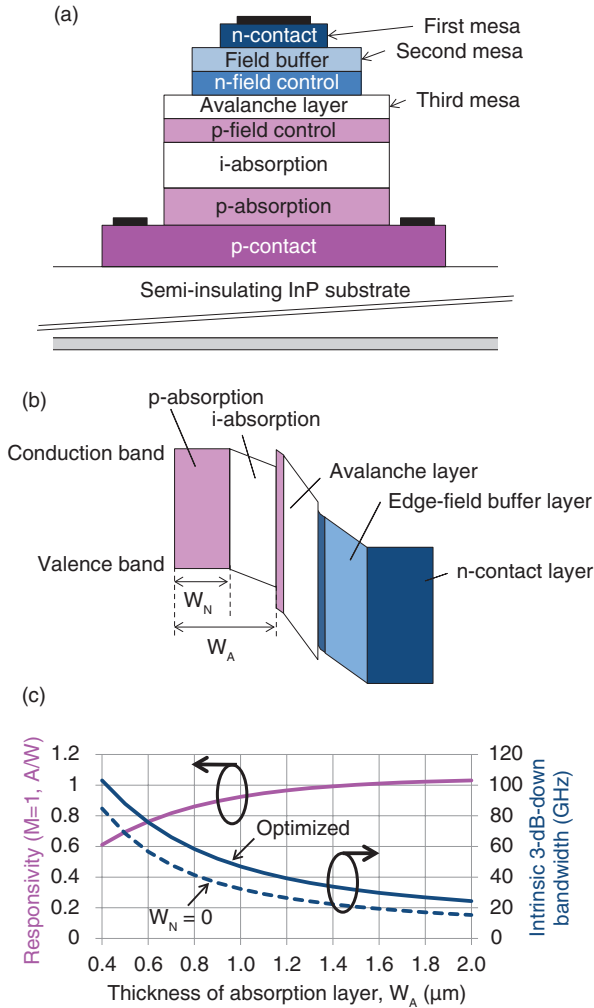
(a)

n-contact — First mesa

Field buffer — Second mesa

n-field control

Avalanche layer — Third mesa

p-field control

i-absorption

p-absorption

p-contact

Semi-insulating InP substrate

(b)

p-absorption

i-absorption

Conduction band

Avalanche layer

Edge-field buffer layer

Valence band

n-contact layer

W_N

W_A

(c)

Fig. 2. (a) Schematic cross section of inverted p-down APD with triple mesa. (b) Parameters for calculation and (c) calculated responsivity (M = 1) and 3-dB-down bandwidth (M = 1), considered only in terms of intrinsic carrier transit time in absorption layer against total thickness of absorption layer.

Table 1. Dimensions of large-area diodes.

	Diode 1	Diode 2	Area ratio
Diameter 1 (1st mesa)	100 μm	200 μm	4.00
Diameter 2 (2nd mesa)	110 μm	210 μm	3.64
Diameter 3 (3rd mesa)	130 μm	230 μm	3.13

sensitivity, we have to optimize the thickness of the avalanche layer to suit the application.

Thus, the thickness of the InAlAs avalanche layer is 0.1 μm, which enables us to obtain a large GBP of 235 GHz [3].

To obtain good stability and reliability, it is important to confine the electric field inside the avalanche layer vertically. To meet this requirement, we generally employ a SACM (separation of absorption, charge, and multiplication) structure [5]. The p-doped and n-doped field-control layers sandwiching the avalanche layer play an important role in confining

the high electric field within the avalanche layer.

The electric field must also be laterally confined to prevent degradation of the semiconductor surface. The electric field affects not only the stability and reliability, but also the bandwidth determined by the CR (capacitance-resistance) time constant because the effective junction area is defined by the confinement of the electric field. Two techniques have been reported for achieving lateral confinement for 10-Gbit/s systems, namely, zinc diffusion [6] and ion implantation [7]. Although they obtained sufficient bandwidth and reliability for 10-Gbit/s operation, the APD structures built using these techniques require a complicated fabrication process. Our inverted p-down APD with triple-mesa structure is promising as a way to overcome this issue.

The triple-mesa structure shown in Fig. 2(a) reduces the intensity of the electric field in the peripheral region of the mesa [8]. All the mesas are formed by conventional wet etching techniques. This mesa structure results in reduced dark current at a mesa surface, which extends the life of the device.

We evaluated the effect of the triple mesa by measuring the ratio of the capacitance-voltage (C-V) curves of two large-area diodes with different dimensions, as listed in **Table 1**. The area-size ratios between two diodes of the first, second, and third mesa were 3.13, 3.64, and 4.00, respectively. The C-V relationship can be expressed simply as

$$C(V) = \varepsilon(V) \, S(V) \, / \, d(V),$$

where ε, S, and d are the dielectric constant, effective area size, and depletion layer thickness, each of which depends on the bias voltage. By taking the ratio of the two C-V curves, the relationship is expressed as

$$C2(V) \, / \, C1(V) = S2(V) \, / \, S1(V).$$

The C-V curves of two diodes are shown in **Fig. 3(a)**. The capacitance ratio versus bias voltage calculated by two C-V curves is shown in **Fig. 3(b)**. The curve has three steps corresponding to the ratios of the three area sizes of the triple-mesa structure. Since the breakdown voltage of this sample is 27.4 V, these results show that the electric field is confined by
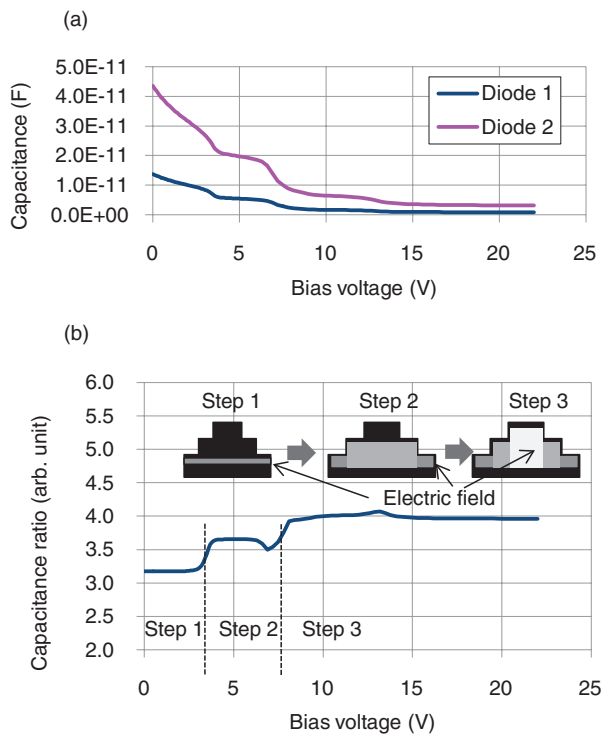
(a)

(b)

Fig. 3. (a) Capacitance vs. bias voltage curves of two diodes and (b) capacitance ratio vs. bias voltage.

the first mesa at the operating condition of M = 10.

The photocurrent distribution across the APD mesa at a bias condition providing an M value of 10 is shown in **Fig. 4**. Light was irradiated from the substrate side, and the optical power was set to −20 dBm. The photocurrent curve has a maximum level from −5 to 5 µm due to reflection from the mirror on the top of the first mesa and the high intensity of the electric field under the first mesa, as mentioned above. The 3-dB-down bandwidth was obtained by measuring the OE (opto-electronic) response at the corresponding point. The measured 3-dB-down bandwidth maintains almost the same value in the first mesa and falls off rapidly toward the outside. This indicates that the electric field is sufficiently high only under the first mesa. These results again demonstrate sufficient confinement of the electric field by the first mesa. The 3-dB-down bandwidth at the center reaches 18 GHz even for an M value of 10. This value is sufficient for 25-Gbit/s applications.
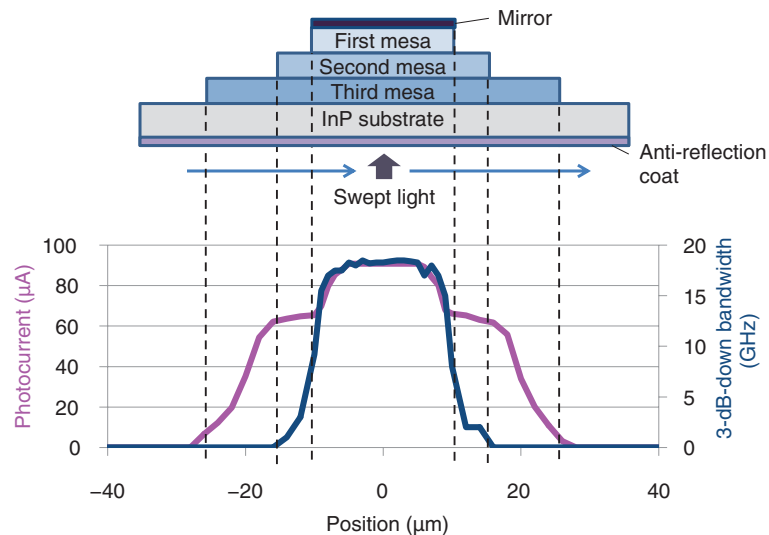

Fig. 4. Cross-sectional profile of photocurrent and 3-dB-down bandwidth against the position of irradiated light.
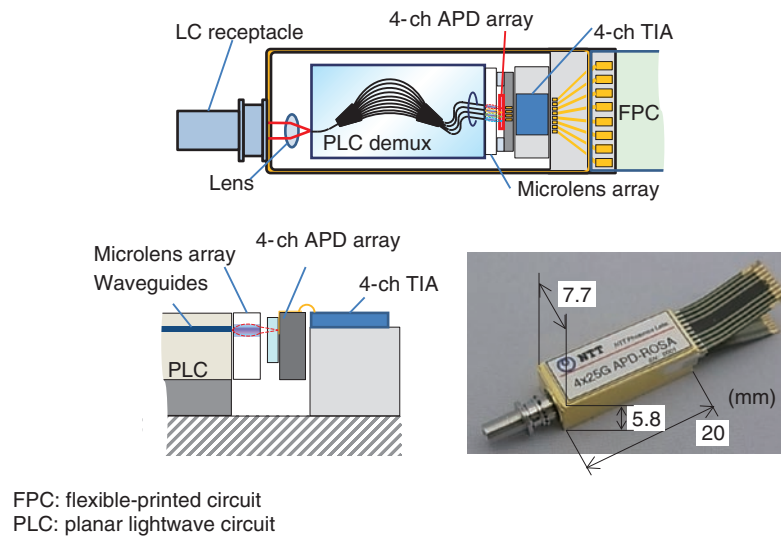
FPC: flexible-printed circuit
PLC: planar lightwave circuit

Fig. 5.   Schematic view and photograph of 4-ch APD-ROSA.

3.   APD-ROSA module for 100-Gbit/s Ethernet systems

Next, we applied our high-speed APD chip to the APD-ROSA. A photograph and schematic illustrations of our 4-ch APD-ROSA are shown in **Fig. 5**. The size of the package body, excluding the LC-type receptacle and FPCs (flexible-printed circuits), is 7.7 × 20 × 5.8 mm. The APD-ROSA includes a monolithic 4-ch APD array, a planar lightwave circuit demultiplexer (PLC demux), a microlens array, and a commercially available 4-ch transimpedance amplifier (TIA) [9, 10]. Our fabricated silica PLC demux has one single-mode input waveguide and four multimode output waveguides, which provide a flat-top spectrum [11]. The APD-array chip was flip-chip mounted on a subcarrier having signal lines for right-angle surface mounting. Since the glass microlens array and APD array on the subcarrier were attached to the output end of the PLC demux chip, the optical coupling distance between the PLC and APD was minimized to a few hundred micrometers.

We measured the back-to-back transmission and the transmission over a 50-km-long single-mode fiber (SMF). The experimental setup is shown in **Fig. 6**. Here, a 25.78-Gbit/s NRZ (non-return-to-zero) on-off keying optical signal consisting of a 2^{31}-1 PRBS (pseudo-random bit sequence) was generated using a tunable laser source and a $LiNbO_3$ Mach-Zehnder (LN) modulator. Wavelengths were set at 1295.56 (lane 0), 1300.05 (lane 1), 1304.58 (lane 2), and 1309.14 nm (lane 3).

Eye diagrams of the electrical output from the APD-ROSA for back-to-back transmission and after 50-km transmission are shown in **Fig. 7(a)**. We obtained clear eye openings for each lane and for both types of transmission. The BER (bit error rate) characteristics are shown in **Fig. 7(b)**, where the back-to-back receiver sensitivity levels were –20.0, –20.3, –20.1, and –20.0 dBm for lanes 0, 1, 2, and 3, respectively. After 50-km transmission, no significant transmission penalties were observed. Negative values of power penalties are explained by the relationship between the positive chirp parameter of the modulator and the normal chromatic dispersion of the 50-km SMF. These results show that our high-speed APD is applicable to APD-ROSAs for 100-Gbit/s systems, and they also indicate the possibility of extending the transmission distance without increasing the power consumption or package size of the receiver module. The APD-ROSA consumes as little as 0.7 W of power and needs no additional space for a preamp. This configuration opens up the possibility of mounting the ROSA in a CFP4 package and of using it in larger capacity Ethernet systems of the future, such as 400-Gbit/s and 1-Tbit/s Ethernet.

4.   Conclusion

We developed an inverted p-down APD with high-speed and stable performance. High responsivity (0.9 A/W), large bandwidth (18 GHz at M = 10), and a

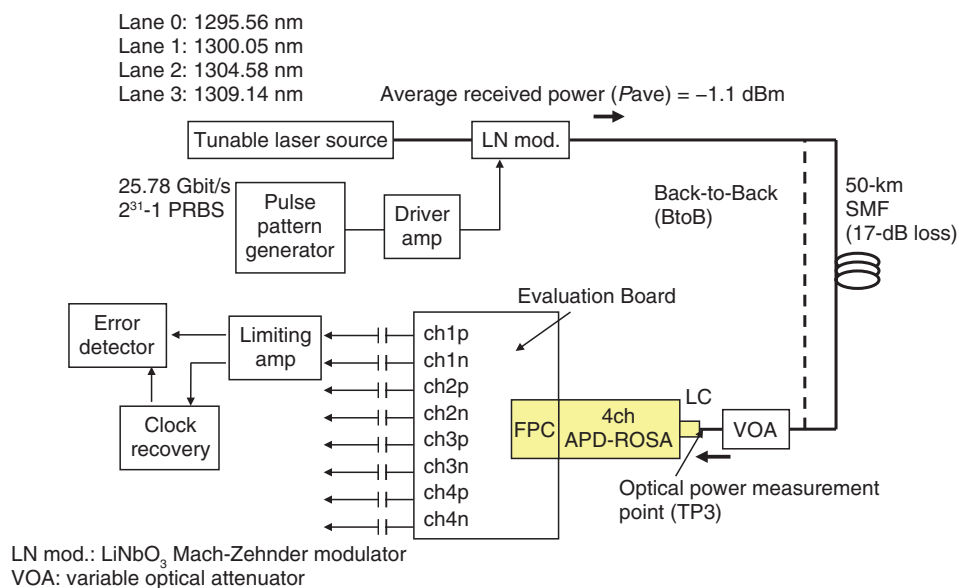Lane 0: 1295.56 nm
Lane 1: 1300.05 nm
Lane 2: 1304.58 nm
Lane 3: 1309.14 nm

Average received power (Pave) = −1.1 dBm

Fig. 6. Experimental setup.

(a)

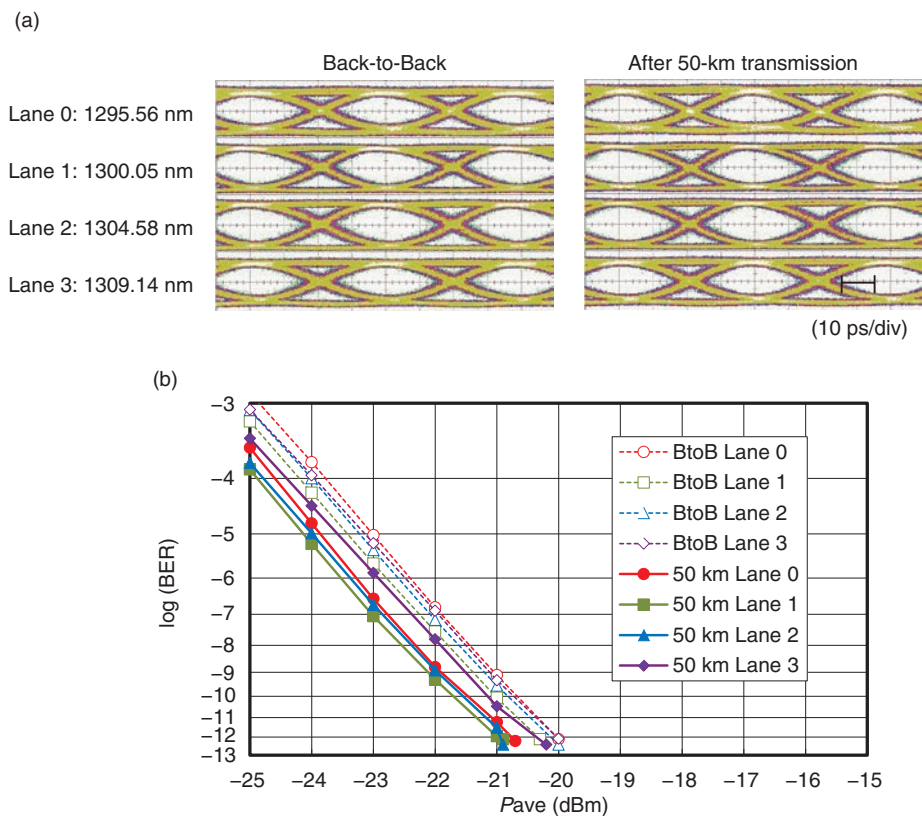|	Back-to-Back	After 50-km transmission
Lane 0: 1295.56 nm		
Lane 1: 1300.05 nm		
Lane 2: 1304.58 nm		
Lane 3: 1309.14 nm		

(10 ps/div)

(b)

Fig. 7. (a) Electrical output waveforms and (b) BER curves for back-to-back and after 50-km transmission.

large GBP (235 GHz) were achieved by optimally designing the absorption layer (1.0 μm) and InAlAs avalanche layer (0.1 μm). The C-V characteristics and photocurrent profile indicate strong confinement of a high electric field in the avalanche layer, which is achieved with two field control layers and a triple-mesa structure.

A 100-Gbit/s (4 × 25-Gbit/s) ROSA using a monolithic four-channel APD array and an ultrasmall PLC demux exhibit minimum receiver sensitivities of –20 dBm and below for back-to-back transmission. We succeeded in achieving 50-km error-free transmission without an optical amplifier. These results indicate that our receiver module technology can contribute to reducing the size and power consumption of optical transceivers toward future 400-Gbit/s and 1-Tbit/s Ethernet multi-wavelength networks.

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