Feature Articles: Device Technology Development for Beyond 100G Optical Transport Network

High Frequency Optical Module Assembly Technique Enabling High Modulation Speed over 100 Gbit/s/λ

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Abstract

A novel optical module assembly technique enabling high modulation bandwidth is described. This optical module features not only high modulation bandwidth but also a small footprint and low-power dissipation. These features help accelerate optical module development for 400-Gigabit Ethernet applications.

Keywords: 100 Gbit/s/λ, high modulation bandwidth, flip-chip interconnection

1. Introduction

In response to the urgent demand for expanded network bandwidth for mobile and cloud computing networks, the standardization of high transmission bandwidth is being actively discussed. In Ethernet standardization, the Institute of Electrical and Electronic Engineers (IEEE) standard 802.3ba [1] was adopted as the standard for 100-Gigabit Ethernet (100GbE) in 2010 (Fig. 1). The IEEE 802.3ba standards define that wavelength-division multiplexing (WDM) transmission technology be utilized to establish 100GbE optical links for 10-km and 40-km single-mode fiber (SMF) transmission. In WDM transmission, four 25-Gbit/s optical data signals with different wavelengths are launched on SMFs and travel along the SMFs. This transmission scheme is called multi-lane transmission.

In 2013, the IEEE 802.3bs [2] task force started discussions on 400-Gigabit Ethernet (400GbE) standards to cover the emerging shortage of bandwidth capacity in 100GbE based networks. The 400GbE transmission uses a multi-lane transmission scheme with a newly introduced signal modulation technology called four-level pulse amplitude modulation (PAM-4)^{*1}. Eight 50-Gbit/s PAM-4 optical signals



Fig. 1. Ethernet standardization trends.

with different wavelengths establish a 400GbE fiber optic link with the multi-lane scheme.

In the optical transceiver marketplace, some manufacturers launched their 400GbE transceiver products,

^{*1} PAM: A form of pulse modulation. By making the amplitude direction multilevel, we can increase the amount of information per modulation. At level four modulation, it is PAM-4: log₂ 4 = 2bit.



Fig. 2. Schematic structure of wire and flip-chip interconnections.

known as CFP8 (centum (100) gigabit form-factor pluggable 8) [3], before the IEEE 802.3bs task force had finalized the 400GbE standards. This CFP8 transceiver typically has four optical assemblies consisting of two transmitter optical subassemblies (TOSA) and two receiver optical subassemblies (ROSA). Each assembly of TOSA and ROSA runs at 200 Gbit/s with four wavelengths and transmits and receives 50-Gbit/s optical signals per wavelength. There are various requirements for cost reduction and downsizing of the CFP8 400GbE optical transceivers arising from an issue involving the use of four optical assemblies. This has made establishing optical assemblies based on serial 100-Gbit/s with one lambda (λ : wavelength) transmission an urgent priority for future 400GbE fiber optic networks.

A new assembly technique developed by the NTT Device Innovation Center can establish a high modulation bandwidth in each wavelength by improving the high-speed electromagnetic characteristics in an optical module with a novel flip-chip interconnection^{*2} technique. With this new technique, each wavelength transmits an optical signal at 100 Gbit/s (100 Gbit/s/ λ), thus enabling 400GbE to be attained. This new assembly technique is explained in detail in the following sections.

2. 100 Gbit/s/λ-high frequency assembly technique

The serial 100 Gbit/s optical signal transmission is a key technology for future Ethernet networks. By using four wavelengths at 100 Gbit/s, the 400GbE transmission can be established. A flat and wideband frequency response for the serial 100-Gbit/s optical module is essential in order to obtain multi-level modulation (PAM-4) and a high-speed symbol rate (50 Gbaud) in the serial 100-Gbit/s optical signal transmission. However, conventional optical transmitter modules cannot extend the modulation bandwidth beyond 50 Gbit/s at high-speed transmission such as 50-Gbit/s operation. The schematic structure of a wire interconnection in the conventional optical transmitter module is shown in Fig. 2(a). The radio frequency (RF) signal is transmitted from an RF substrate through a wire to an electroabsorption modulator (EAM) integrated with a distributed feedback laser (EAM-DFB laser, or EA-DFB laser). Due to the nature of the characteristics in wire inductance, the modulation bandwidth degrades rapidly with a longer wire.

^{*2} Flip-chip interconnection: A chip interconnection technique. Generally, by forming small protruding metallic terminals as electrodes of chips, the chips can be placed and connected on to the face of the substrates. This helps to reduce the assembly footprint compared to conventional metal wire interconnection techniques.

To resolve this issue, we propose using a flip-chip interconnection technique as a wire-free interconnection. The schematic structure of the flip-chip interconnection is shown in **Fig. 2(b)**. A flip-chip bonding substrate is connected to an RF substrate and an EAM with gold (Au) bumps. The height of the Au bumps is as small as just a few micrometers (~10 μ m). To eliminate wire connections between the EAM and a terminator, a terminator resistance thin film is integrated on the flip-chip bonding substrate. The flip-chip interconnection reduces the parasitic inductance since the wire is no longer necessary. Therefore, the flip-chip interconnection improves the frequency response of the module, as shown in **Fig. 3**.

Eye diagrams of 56-Gbaud PAM-4 (112 Gbit/s) signals obtained under the configuration of a back-toback transmission and after 10-km SMF transmission using the flip-chip interconnection EA-DFB laser module are shown in **Fig. 4**. Clear eye opening characteristics with four levels (0, 1, 2, 3) are observed even after 10-km SMF transmission thanks to the high modulation bandwidth and the flat frequency response of the module.

Generally, the digital signal processing circuits are introduced to high-speed optical communication systems using a multi-level modulation format in order to compensate for the bandwidth degradation occurring in the optical modules. However, those digital signal processing circuits use a lot of electric power, which creates additional latency on the transmission link, so it is desirable to reduce the number of digital signal processing circuits for future Ethernet networks.

The bit error rate (BER) characteristics are shown in Fig. 5 for back-to-back configuration and 10-km SMF transmission without any digital signal processing such as BCH (Bose-Chaudhuri-Hocquenghem) forward error correction (FEC). The BER of less than 1×10^{-3} , which is the error-free condition for the BCH FEC, was obtained even after 10-km SMF transmission. Our optical module has a sufficiently high modulation bandwidth and flat frequency response to make the digital signal processing unnecessary [4]. The module enables us to construct lowpower consumption and low-latency networks thanks to the elimination of the digital signal processing circuits. Moreover, this optical module helps reduce the number of wavelengths from eight to four so that we can establish 400GbE transmission.

Moreover, if digital signal processing is utilized to compensate for the bandwidth degradation in an optical transmission link while using our optical module,



Fig. 3. Frequency response of wire and flip-chip interconnections.



Fig. 4. Eye diagrams under 56-Gbaud PAM-4 operation.

dramatic improvements in transmission bandwidth can be expected. In our experimental work, we demonstrated 200-Gbit/s per wavelength operation [5]. By applying this technique in 100-Gbit/s per wavelength operation, the digital signal processing as a bandwidth degradation compensator becomes unnecessary, which thus reduces power consumption.

3. Future plans

The proposed assembly technique makes it possible to achieve a smaller optical module with lower-power consumption. We plan to create a flip-chip interconnection 4ch optical transmitter module integrated with an optical multiplexer for 400GbE transmission.



Fig. 5. BER characteristics under 56-Gbaud PAM-4 operation.

References

- [1] Website of IEEE standard 802.3ba Ethernet Task Force, http://www.ieee802.org/3/ba/
- [2] Website of IEEE standard 802.3bs Ethernet Task Force, http://www.ieee802.org/3/bs/
- [3] Website of the CFP Multi-Source Agreement, Documents, http://www.cfp-msa.org/documents.html
- [4] S. Kanazawa, T. Fujisawa, K. Takahata, Y. Nakanishi, H. Yamazaki, Y.

Ueda, W. Kobayashi, Y. Muramoto, H. Ishii, and H. Sanjoh, "56-Gbaud 4-PAM (112-Gbit/s) Operation of Flip-chip Interconnection Lumped-electrode EADFB Laser Module for Equalizer-free Transmission," Proc. of the Optical Fiber Communication Conference and Exhibition (OFC) 2016, W4J.1, Anaheim, CA, USA, Mar. 2016.

[5] S. Kanazawa, H. Yamazaki, Y. Nakanishi, T. Fujisawa, K. Takahata, Y. Ueda, W. Kobayashi, Y. Muramoto, H. Ishii, and H. Sanjoh, "Transmission of 214-Gbit/s 4-PAM Signal Using an Ultrabroadband Lumped-electrode EADFB Laser Module," Proc. of OFC 2016, Th5B.3, Anaheim, CA, USA, Mar. 2016.



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