Indium Phosphide-based Heterojunction Bipolar Transistors with Metal Subcollector Fabricated Using Substrate-transfer Technique

Yuta Shiratori, Takuya Hoshi, Norihide Kashio, Kenji Kurishima, and Hideaki Matsuzaki

Abstract

We fabricated indium phosphide (InP)-based heterojunction bipolar transistors (HBTs) with a highly thermal conductive gold (Au) subcollector on a silicon carbide substrate using a substrate-transfer technique. The fabricated HBTs show good electrical characteristics without any degradation caused by the transfer process. In addition, they exhibit about a 50% reduction in thermal resistance (R_{th}) compared with conventional HBTs on an InP substrate. The reduced R_{th} enables us to increase collector current density without a rise in the junction temperature of HBTs, which improves the HBT high-frequency performance. The fabricated Au-subcollector HBTs have great potential for boosting the operation speed of future telecommunications integrated circuits.

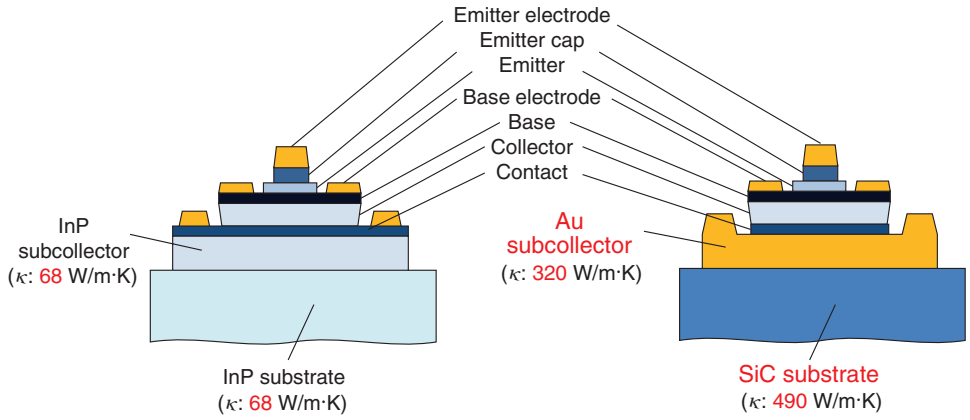
Keywords: InP-based HBT, thermal resistance, wafer bonding

1. Introduction

Indium phosphide (InP)-based heterojunction bipolar transistors (HBTs) have excellent high-frequency performance suitable for large-bandwidth integrated circuits (ICs). Increasing the current density of HBTs is very effective for improving the operating speed of these ICs because the increased current density helps to reduce the charging time. We demonstrated a current-gain cutoff frequency of 513 GHz and a maximum oscillation frequency of 637 GHz for a 0.25-μm-wide-emitter HBT at the collector current density (J_C) of 9.5 mA/μm^2 [1]. However, the increased current density results in higher power consumption per unit area, which leads to a rise in junction temperature and degraded current gain of the HBTs.

To suppress these undesirable effects, it is necessary to improve the heat transfer from inside the HBTs to the backside of the substrate. A basic approach to suppressing them is to thin the substrate or change the substrate to one with high thermal conductivity. However, drastically improving the heat transfer is a major challenge because of the possible degradation of the electrical performance associated with the fabrication process.

To improve the heat transfer, we propose a novel HBT structure with a gold (Au) subcollector fabricated on a silicon carbide (SiC) substrate using a substrate-transfer technique. The proposed HBT successfully suppresses the degradation of the current gain at high current density by reducing the thermal resistance, thanks to the highly thermal conductive SiC substrate and the simultaneously introduced highly thermal conductive Au subcollector.



(a) Conventional HBT on InP substrate (b) Metal-subcollector HBT

Fig. 1. Cross-sectional view of (a) conventional InP-based HBT on InP substrate and (b) metal-subcollector HBT on SiC substrate.

2. Device structure and fabrication process

A cross-sectional view of the proposed HBT structure is shown in **Fig. 1**. For comparison, a conventional InP-based HBT structure is also shown. The conventional HBTs are formed on an InP substrate, and the subcollectors are also made of InP. In contrast, the substrate for the proposed HBT is SiC, and the subcollectors are not a semiconductor but a metal (Au). We therefore call the proposed HBT a metal-subcollector HBT. Because SiC and Au have much higher thermal conductivity (490 and 320 $Wm^{-1}K^{-1}$, respectively) than InP (68 $Wm^{-1}K^{-1}$), metal-subcollector HBTs can enhance the heat transfer compared with HBTs on an InP substrate. In addition, the collector current of metal-subcollector HBTs flows vertically through an indium gallium arsenide (InGaAs) contact layer because the Au subcollector also acts as a collector electrode. This is a clear advantage for heat transport in the metal-subcollector HBTs because the thickness of the InGaAs contact layer, which has very low thermal conductivity of 5 $Wm^{-1}K^{-1}$, can be reduced without increasing its electrical resistance.

The epitaxial layers for metal-subcollector HBTs are designed for high-current-density operation (> 10 $mA/\mu m^2$). In addition, we prepared three kinds of HBTs with different collector contact layer (t_{cc}) thicknesses (50, 30, or 0 nm) to investigate the effect of the thickness of the InGaAs t_{cc} on the thermal resistance (R_{th}) of HBTs. The emitter is 20-nm-thick InP. The gallium arsenide antimonide (GaAsSb) base is 30 nm thick and highly C-doped at 8×10^{19} cm^{-3} (for t_{cc} of 50 nm) or 4×10^{19} cm^{-3} (for t_{cc} of 30 and 0 nm). The collector is 100-nm-thick InP.

The fabrication process of HBTs started with the epitaxial growth of HBT layers on a 3-inch InP substrate by metal-organic chemical vapor deposition. After Au was deposited as an adhesive and subcollector material on both the HBT layers and a 3-inch SiC substrate, they were bonded using a surface activated bonding (SAB) method as shown in **Fig. 2(a)**. SAB prevents thermal degradation of the epitaxial layers due to the sufficiently low bonding temperature (~150°C) [2]. Note also that the growth sequence of the epitaxial-layer structure was inverted for the wafer bonding, which started from the emitter cap layer.

A scanning acoustic microscope image of the bonded wafer is shown in **Fig. 3(a)**. The InP and SiC substrates were bonded with almost no voids except at the wafer edge, thanks to the excellent physical properties of Au (low Young's modulus and non-oxidizing). After the removal of the InP substrate as shown in **Fig. 2(b)**, HBT epitaxial layers were completely transferred onto the SiC substrate as shown in **Fig. 3(b)**. Finally, HBTs with an emitter width of 0.25 μm were fabricated using the SiO_2/SiN (silicon dioxide/silicon nitride) sidewall process [3] as shown in **Fig. 2(c)**. A scanning electron microscope image of a fabricated metal-subcollector HBT with an emitter size of 0.25 μm × 4.0 μm is shown in **Fig. 4**. HBTs were successfully fabricated on a SiC substrate without any serious problems related to the bonding process.

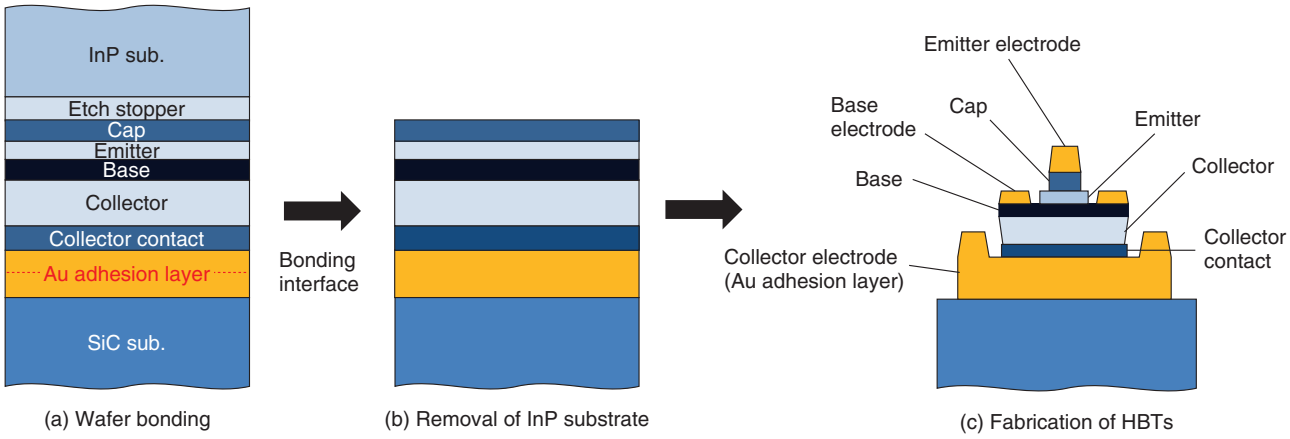
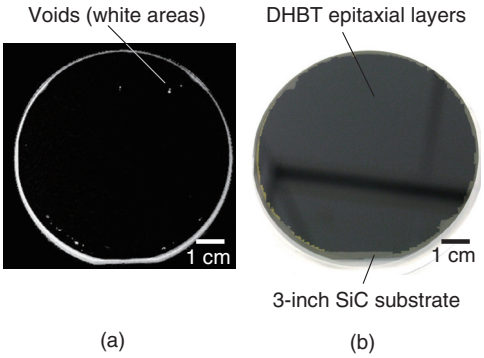


Fig. 2. Fabrication steps for metal-subcollector HBT.



DHBT: double heterojunction bipolar transistor

Fig. 3. (a) Scanning acoustic microscope image of HBT epitaxial layers on an InP substrate bonded to an SiC substrate. (b) Photograph of the bonded wafer after removal of InP substrate.

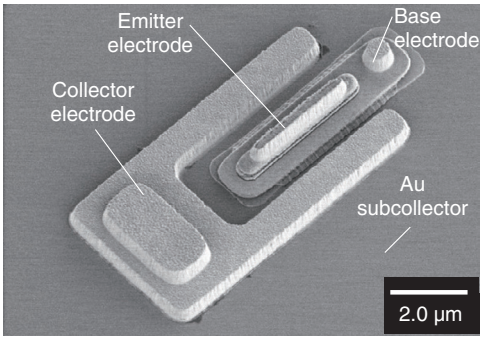


Fig. 4. Scanning electron microscope image of a fabricated metal-subcollector HBT with an emitter size of 0.25 μm × 4.0 μm.

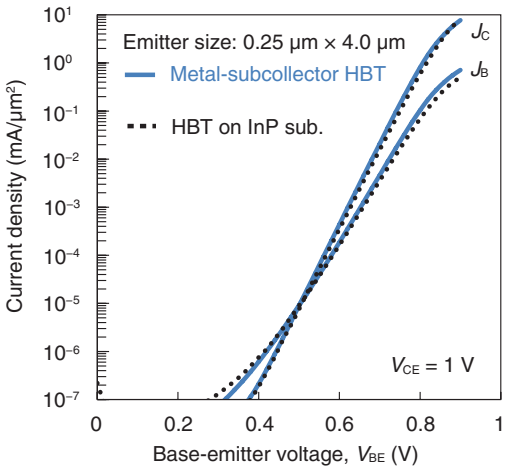
3. Device characteristics

We measured the electrical characteristics of the fabricated HBTs to investigate how the bonding process affected the HBTs. Gummel plots for the metal-subcollector HBT on a SiC substrate (hereinafter referred to as an HBT on SiC) with a 50-nm-thick InGaAs collector contact layer are shown in **Fig. 5**. For comparison, Gummel plots for a conventional HBT on an InP substrate (hereinafter referred to as an HBT on InP) with the same epitaxial layer structure are also shown (black dotted lines). As seen in the graph, the two HBTs had almost the same current-transfer characteristics. We confirmed from high-frequency measurements that the HBT on SiC exhibits a current-gain cutoff frequency of 337 GHz and a maximum oscillation frequency of 400 GHz at J_C of 15 mA/μm^2. These values are comparable to those of the HBT on InP. These results indicate that the carrier transport properties were not degraded by the bonding process.

Next, to investigate heat transport properties, we estimated the R_{th} for the HBTs from the electrical characteristics in a common-base configuration. R_{th} is expressed by the following equation [4].

$$R_{th} = \frac{1}{\phi}\frac{\Delta V_{BE}}{\Delta P},$$

where ΔV_{BE} is a voltage shift in the base-emitter voltage for a given collector current when the collector-base voltage increases, ΔP is an associated increase in power dissipation, and ϕ is a thermo-electric feedback coefficient, experimentally obtained from the



J_C: collector current density
J_B: base current density

Fig. 5. Gummel plots of fabricated HBTs.

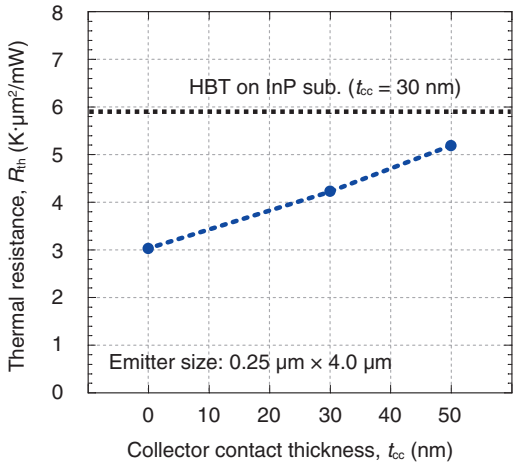


Fig. 6. Thermal resistance as a function of collector contact thicknesses of fabricated HBTs.

Gummel plots at various ambient temperatures. For the InP/GaAsSb HBTs, the measured ϕ is about 0.9 mV/K. In this article, the R_{th} is normalized by the total emitter junction area.

The R_{th} as a function of t_{cc} for an HBT on SiC is plotted in **Fig. 6**. For comparison, the R_{th} of an HBT on InP with t_{cc} of 30 nm is also plotted (black dotted line). When t_{cc} is 30 nm, R_{th} for the HBT on SiC is about 30% lower than that for the HBT on InP due to the effect of the highly thermal conductive SiC substrate and Au subcollector. In addition, the R_{th} for the HBT on SiC decreases with t_{cc}. In particular, the HBT on SiC without the InGaAs contact layer (t_{cc} = 0 nm) exhibits R_{th} of 3.02 Kμm^2/mW, which is about a 50% reduction compared to the HBT on InP. The obtained R_{th} values are reasonable compared with those estimated from the analytical model of R_{th} [5]. It is expected that the R_{th} can be further reduced by optimizing the thickness of the Au subcollector and utilizing substrates with higher thermal conductivity such as diamond.

Collector *I-V* curves for the HBTs without the InGaAs contact layer (t_{cc} = 0 nm) on SiC are shown in **Fig. 7**. Junction temperatures (T_j) were estimated from the measured R_{th} and are plotted as dotted curves. Due to the reduced R_{th}, the T_j of the HBT on SiC is less than about half that of the HBT on InP. As a result, the former successfully suppresses a reduction in current-gain in the high-V_{CE} and high-I_C bias regions (~20 mW/μm^2). The proposed HBT is therefore very effective for increasing the operation current density without degradation of the current gain due to device self-heating.

4. Summary

We fabricated InP-based HBTs with a Au subcollector on a SiC substrate using the substrate-transfer technique. From a comparison of electrical characteristics between the metal-subcollector HBT on SiC and a conventional HBT on an InP substrate, we confirmed that the wafer-bonding process did not degrade the carrier transport properties of the HBT. In addition, the HBTs on the SiC substrate exhibited about a 50% reduction in R_{th} compared with those on the InP substrate. The proposed metal-subcollector HBT technology is very promising for improving the speed performance of ICs to support future large-capacity telecommunications network systems.

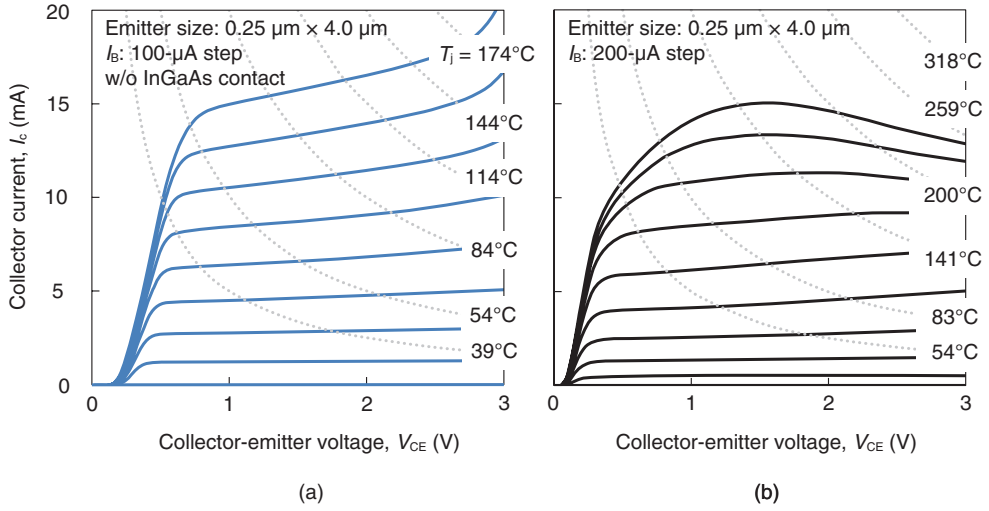


Fig. 7. I_C-V_{CE} characteristics of HBTs fabricated on (a) SiC substrate and (b) InP substrate. Dotted lines show junction temperatures estimated from R_{th}.

References

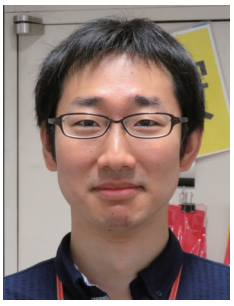
[1] N. Kashio, T. Hoshi, K. Kurishima, M. Ida, and H. Matsuzaki, "Improvement of High-frequency Characteristics of InGaAsSb-base Double Heterojunction Bipolar Transistors by Inserting a Highly Doped GaAsSb Base Contact Layer," IEEE Electron Device Lett., Vol. 36, No. 7, pp. 657–659, 2015.

[2] Y.-H. Wang, J. Liu, and T. Suga, "Low-temperature Wafer Bonding Using Gold Layers," Proc. of ICEPT-HDP '09 (International Conference on Electronic Packaging Technology & High Density Packaging), pp. 516–519, Beijing, China, Aug. 2009.

[3] N. Kashio, K. Kurishima, M. Ida, and H. Matsuzaki, "Over 450-GHz f_t and f_{max} InP/InGaAs DHBTs with a Passivation Ledge Fabricated by Utilizing SiN/SiO_2 Sidewall Spacers," IEEE Trans. Electron Devices, Vol. 61, No. 10, pp. 3423–3428, 2014.

[4] W. Liu, "Handbook of III-V Heterojunction Bipolar Transistors," p. 363, Wiley-Interscience, New York, 1998.

[5] F. N. Masana, "A New Approach to the Dynamic Thermal Modeling of Semiconductor Packages," Microelectron. Reliab., Vol. 41, No. 6, pp. 901–912, 2001.



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