

## Effective Compression of Quantum Braided Circuits Aided by ZX-Calculus

### 1. Introduction

Researchers at the National Institute of Informatics (NII) and NTT proposed a compression method for reducing the resources associated with large-scale fault-tolerant quantum circuits that brings practical quantum computation one step closer to reality.

A major technical challenge for achieving practical quantum computation comes from the very need for a large number of physical qubits to prevent errors from accumulating during that computation. The consequence of this is that a fault-tolerant quantum circuit for a given computation requires a huge amount of resources, both in terms of qubits and computational time. In this work, published in *Physical Review X* on the 11th of November 2020 [1], they designed an efficient method of compressing such circuits with the purpose of decreasing their hardware demands. They used ZX-calculus as an intermediate language to reduce both the number of qubits and time required to execute such computation in many different circuits. With their method, they found an improvement of a 40% compression rate with respect to previous reductions, yielding compression rates higher than 70%. This method promises to open new venues of research in large-scale quantum computing and bring quantum computation closer to reality by relaxing its hardware demands.

### 2. Background

The fast-paced development of quantum technology has brought quantum computing into the era of noisy intermediate-scale quantum (NISQ) devices, which have served as the platform for early proof-of-principle experiments. However, they are still prone to errors, which significantly accumulate during their operation. To obtain a truly practical quantum advantage, the design of a fully operational large-scale

quantum computer with high-error tolerance is required. Current cutting-edge technology allows us to engineer NISQ devices with approximately 100 qubits, while fault-tolerant computers are expected to require millions of physical qubits at least to encode the logical information with sufficiently low error rates. This difference in size is currently the main obstacle to the development of large-scale fault-tolerant quantum computers.

Progress in hardware technology is expected to bring scalability into quantum computer chip manufacturing and qubit controls. However, it is also possible for software to reduce the cost associated with fault-tolerant quantum computation implementations. Large-scale quantum computers will consist of many technological layers from the application level all the way down to the hardware, which will require various rounds of compilation and optimization. The resource cost will then come from the layers where quantum error correction codes are introduced to provide fault-tolerance for the implementation of the circuit. For most current quantum-computer architectures, topological error-correcting codes are preferred, in particular the surface code is expected to be used for superconducting-qubit-based quantum computers where lattice-surgery or braiding is chosen for logical gate operations, the latter being ideally suited to distributed quantum computation. A fault-tolerant implementation of quantum computational circuits not only makes the quantum computer larger but also the runtime longer. “These operations require a high level of external control over quite an extended time. In turn, this means the computation is more susceptible to errors,” says Michael Hanks from NII. Therefore, the possibility of compressing quantum circuits at the logical level not only implies a huge saving for the time and resources needed for quantum computation but also lower errors. “Once a quantum algorithm or computation is compiled into a fault-tolerant

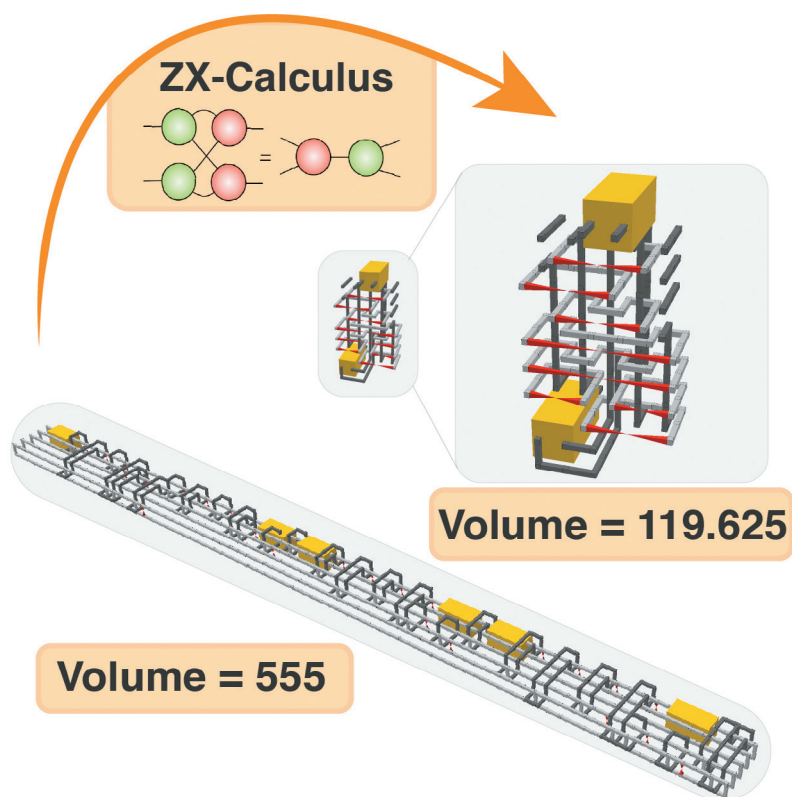


Fig. 1. Compression of a quantum circuit with a 77.4% reduction rate.

circuit, to reduce both the amount of time and space required is paramount to bring practical quantum computers closer to reality,” says Marta Estarellas from NII. Thus far, there has been no established approach to tackle this problem, and effective methods to treat these logical gate circuits have not been formulated.

### 3. Research results

As mentioned above, their method is used for compressing braided fault-tolerant circuits on the three-dimensional (3D) topological code. Braided circuits are generally represented as 3D structures, a low-level close-to-hardware language whose main elements consist of tubes or pipes that represent the defects or logical qubits. A quantum gate circuit can be represented as interlacing pipes. By manipulating these pipes, the quantum gate circuit can be compressed. The main problem in braided circuit reduction is that there are few ad-hoc rules to manipulate these pipes. The first piece of this puzzle is to use ZX-calculus, a language that is equipped with a com-

plete set of rules to manipulate logical gate circuits, to carry out this compression. However, we still need to solve another piece of the puzzle to harness ZX-calculus, and that is discovering the translation relations between ZX-calculus and the components of the braided circuit. The researchers have shown that these two representations of logical gate circuits can be mapped one to another by identifying a new interpretation hidden in ZX-calculus. After testing their compression method against a set of test circuits, they were able to reduce those circuit volumes by approximately 70% on average (**Fig. 1**).

Their method also allows unification of the two main operation models used in surface-code-based computation: lattice-surgery and braiding. “This unification promotes ZX-calculus from a representation of quantum logical circuits to a quantum computer language. We can now think about designing computer languages and compilers in the logical operation layer of the technological stack,” says William J. Munro from NTT. Importantly, the unification of these two models also contributes directly to compression. Taking the hybrid compilation approach,

we can compress a circuit further, beyond what each individual method had achieved.

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#### 4. Methods

Previous methods for fault-tolerant quantum circuit compression have suffered from the complexity of trying to reduce circuits directly in the 3D representation. One of the key contributions of this new method is the inclusion of ZX-calculus as an intermediate language to minimize the circuit volume. This diagrammatic language can be used to represent quantum processes and circuits in the form of tensor networks with a limited set of elements or nodes. This language can then apply a set of transformation rules (axioms) to change the structure of the network without modifying its underlying mathematical meaning (hence its operation). These transformation rules can be carefully applied in such a way that the total number of nodes is reduced. As the set of transformations is complete, any minimal structure can be reached in principle. The compressed circuit in ZX-calculus is then mapped to the braided circuit by applying the newly identified relation between them.

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#### 5. Outlook

Global efforts are pushing quantum technology ahead rapidly with a steadily increasing number of qubits present in each next-generation chip. Nevertheless, in the race to achieve practical quantum computing, it is not enough to just improve the hardware. Software techniques can significantly reduce the requirement for quantum computer hardware, which can bring the development of fault-tolerant quantum computers forward by years. “The logical gate layer situates in the middle of the quantum computer technology stack, and our method can serve as a basis to further develop instruction set architectures and design quantum compliers,” adds Kae Nemoto from NII.

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#### 6. Funding

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#### Reference

- [1] M. R. Hanks, M. P. Estarellas, W. J. Munro, and K. Nemoto, “Effective Compression of Quantum Braided Circuits Aided by ZX-Calculus,” *Phys. Rev. X*, Vol. 10, No. 4, 041030, Nov. 2020.

## Researcher's comment

**What is a Compiler for Error-tolerant Quantum Computers?**

Kae Nemoto

Global Research Center for Quantum Information Science, Principles of Informatics Research Division, National Institute of Informatics

When processing information in a quantum computer, the information is stored in a collective quantum state formed on many qubits. Unfortunately, quantum states are fragile, meaning that the quantum information processes in a quantum computer are heavily affected by noise. Therefore, to increase the size of quantum computers and solve difficult problems over a long period, it is necessary to make them robust to such errors. Quantum computers that are robust to such errors are called fault-tolerant quantum computers (FTQCs). They are the long-term goal for the development of quantum computers, and it is currently an extremely active research field. In an FTQC, information processing is implemented by first creating logical qubits using a quantum error correction code, then implementing fault-tolerant logical quantum gates on those logical

qubits. Generally, FTQCs require a great deal of physical resources to implement quantum gates in a fault-tolerant manner, as well as to encode the information on logical qubits. Naturally, an FTQC is a very big device, hence any saving in resources can have a profound effect in its development.

In collaboration with NTT Basic Research Laboratories, we have used ZX-calculus to design a method to compress quantum circuits. By using this new method for subroutine quantum circuits, we have made it possible to speed up fault-tolerant quantum computation and significantly reduce the resources it requires. This research not only accelerates the implementation of FTQCs but also proposes a new approach to quantum computer languages, which is at the core of compiler design. Our work will provide the foundation for the future development of quantum computer compiler design and quantum computer languages.



## Researcher's comment

**Quantum Circuit Compression of an Error-tolerant Quantum Computer**

William John Munro

Theoretical Quantum Physics Research Group & Research Center for Theoretical Quantum Physics, Quantum Science and Technology Laboratory, NTT Basic Research Laboratories

The principles of quantum mechanics are expected to enable new forms of information and communication technology (ICT) and bring about revolutionary development in the current ICT. It is expected that the development of such quantum devices will be able to solve problems that are difficult or even impossible to achieve with current technologies. To date, NISQ devices with 50 to 100 qubits have been developed. The letter “N” in the word NISQ means noisy, so as the name implies it is a noisy quantum device. It has already been shown that these NISQ devices can create complexity that is extremely difficult to achieve on our traditional computers. However, the presence of noise also means that there is a significant limitation in the quantum computational tasks that can be performed; large and/or difficult problems requiring significant numbers of qubits cannot be solved. To avoid this limitation, it is necessary to develop an FTQC. The development of these FTQCs is believed to be the ultimate future computational goal where they will be able to solve unimaginably difficult prob-

lems. It however requires millions of times as many qubits as today's NISQ device. It is critical to bridge the large gap between today's NISQ devices and tomorrow's FTQCs. In November 2020, we proposed a quantum circuit compression



method for FTQCs that dramatically reduces the number of logical qubits (thus physical qubits) required to execute a given quantum program. Lowering of these resources brings the development of FTQCs significantly forward, and the results were published in the American Physical Society journal Physical Review X. One of the advantages of our method is that it is easy to automate the quantum circuit compression with the resulting circuit naturally verified.

This work was a joint research project with Dr. Michael Hanks, Dr. Marta Estarellas, and Professor Kae Nemoto from the National Institute of Informatics. It was supported by the MEXT Quantum Leap Flagship Program. Researchers from a wide variety of disciplines, including physics, engineering, computer science, and chemistry, are participating in this research. I think that the method we have developed will stimulate the further development of quantum computer design.

**For inquiries:**

Public Relations, NTT Science and Core Technology Laboratory Group

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